# Ironwood Electronics

CSP Interconnect

Measurement and Model Results

prepared by

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10/26/04

## *Table of Contents*

## *Objective*

The objective of these measurements is to determine the rf performance of a CSP interconnect. For G-S-G configurations, a signal pin surrounded by grounded pins is selected for the signal transmission. For G-S-S-G configurations, two adjacent pins are used with all other pins grounded. Measurements in both frequency and time domain form the basis for the evaluation. Parameters to be determined are pin capacitance and inductance of the signal pin, the propagation delay, and the attenuation to 40 GHz.

## *Methodology*

Capacitance and inductance for the equivalent circuits were determined through a combination of measurements in time and frequency domain. Frequency domain measurements were acquired with a network analyzer (HP8722C). The instrument was calibrated up to the end of the 0.022" diameter coax probe. The probe was then connected to the fixture and the response measured from one side of the array. When the pins terminate into an open circuit, a capacitance measurement results. When a short circuit compression plate is used, inductance can be determined.

Time domain measurements are obtained via Fourier transform from VNA tests. These measurements reveal the type of discontinuities at the interfaces plus contacts and establish bounds for digital system risetime and clock speeds.

**Test procedures**

To establish capacitance of the signal pin with respect to the rest of the array, a return loss calibration is performed. Phase angle information for S11 is selected and displayed. When the array is connected, a change of phase angle with frequency can be observed. It is recorded and will be used for determining the pin capacitance.

The self-inductance of a pin is found in the same way, except the CSP contact array is compressed by a metal plate instead of an insulator. Thus a short circuit at the far end of the pin array results. Again, the analyzer is calibrated and S11 is recorded. The inductance of the connection can be derived from this measurement.

**Setup**

Testing was performed with a test setup that consists of a brass plate that contains the coaxial probes. The DUT is aligned and mounted to that plate. The opposite termination is also a metal plate with coaxial probes, albeit in the physical shape of an actual device to be tested.

Figs. 1 and 2 show a typical arrangement base plate and DUT probe:

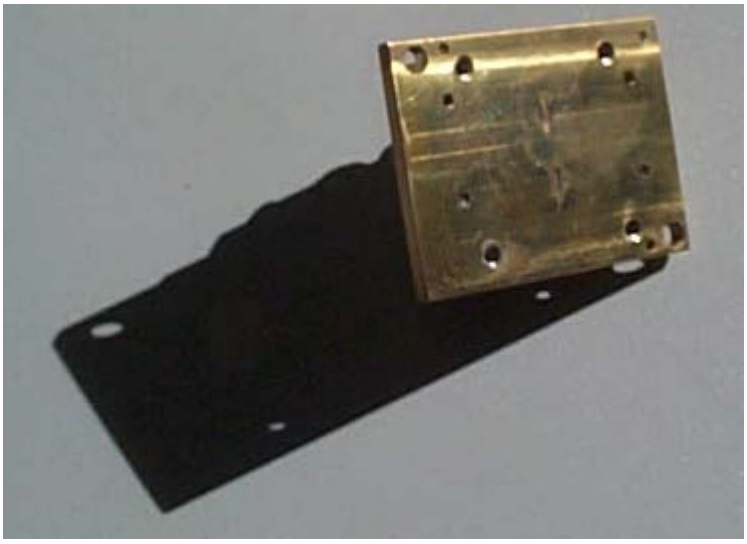

Figure 1 CSP interconnect base plate example

Figure 2 DUT plate

The CSP interconnect and base plate as well as the DUT plate are then mounted in a test fixture as shown below in Fig. 3:

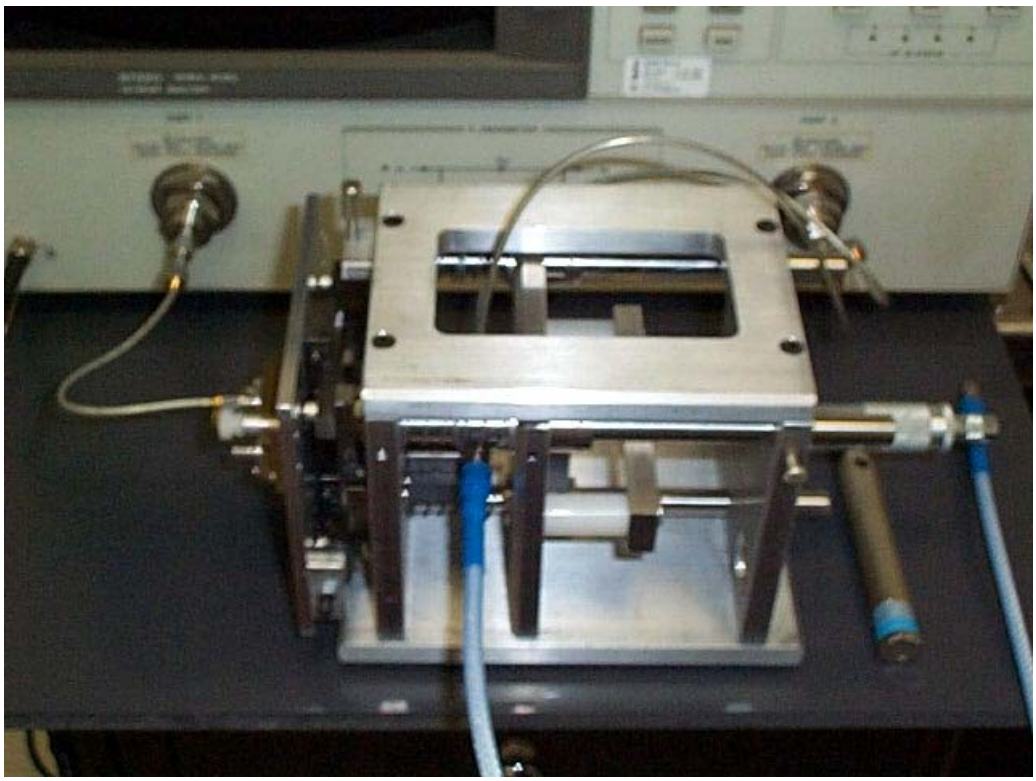

Figure 3 Test fixture

This fixture provides for independent X,Y and Z control of the components relative to each other. X, Y and angular alignment is established once at the beginning of a test series and then kept constant. Z alignment is measured via micrometer and is established according to specifications for the particular DUT.

Connections to the VNA are made with high quality coaxial cables with K connectors.

For G-S-S-G measurements, the ports are named as follows:

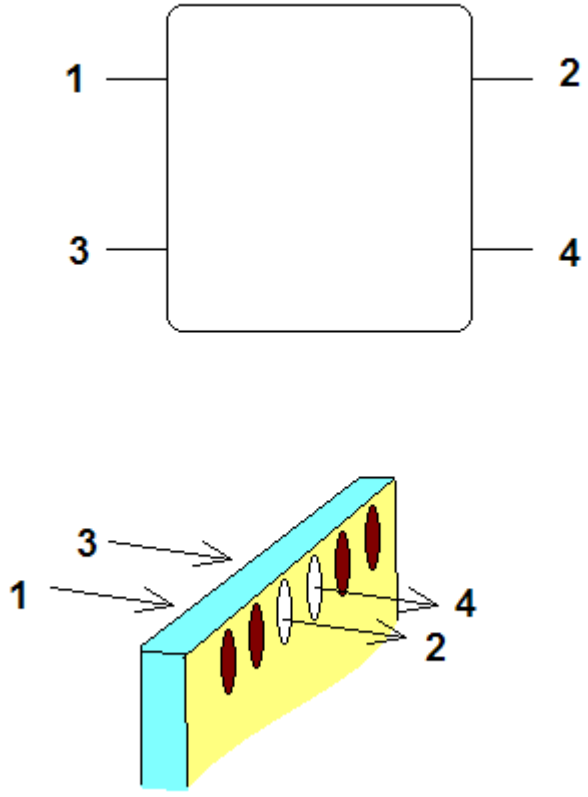


Figure 4  Ports for the G-S-S-G measurements

Signals are routed though two adjacent connections (light areas), unused connections are grounded (dark areas).

## *Measurements G-S-G*

### Time domain

The time domain measurements will be presented first because of their significance for digital signal integrity. TDR reflection measurements are shown in Figs. 5 to 7.

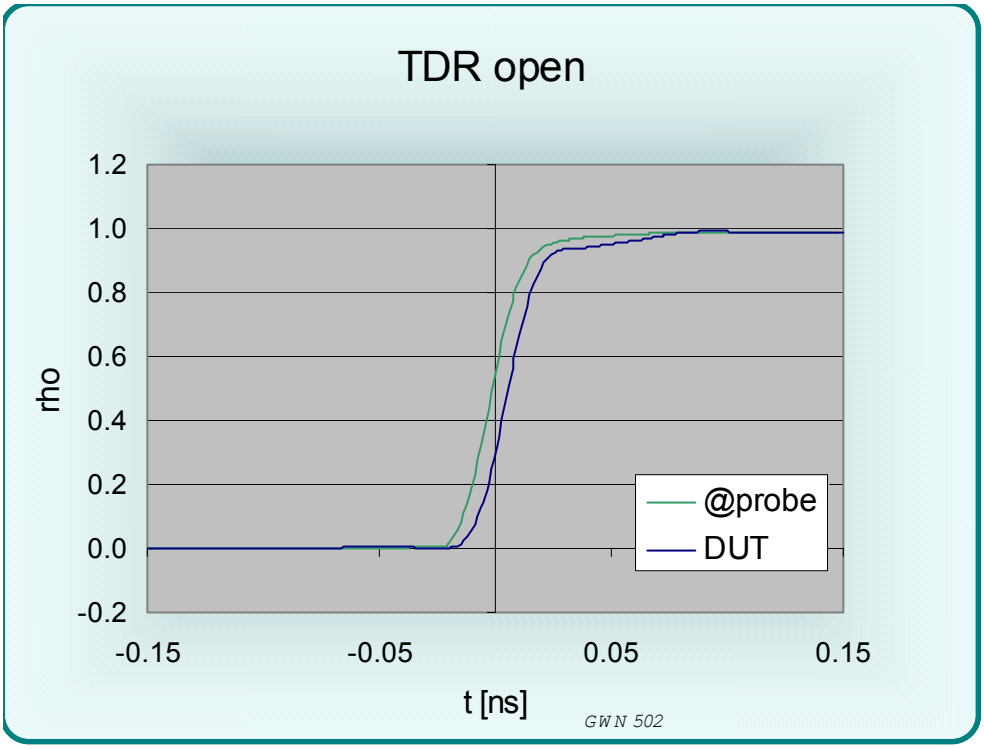


Figure 5 TDR signal from an OPEN circuited CSP interconnect

The reflected signals from the CSP interconnect (rightmost traces) show only a small deviation in shape from the original waveform (leftmost trace). The risetime is about 28.5 ps and is the same as that of the system with the open probe (28.5 ps). Electrical pin length is about 3.0 ps one way.

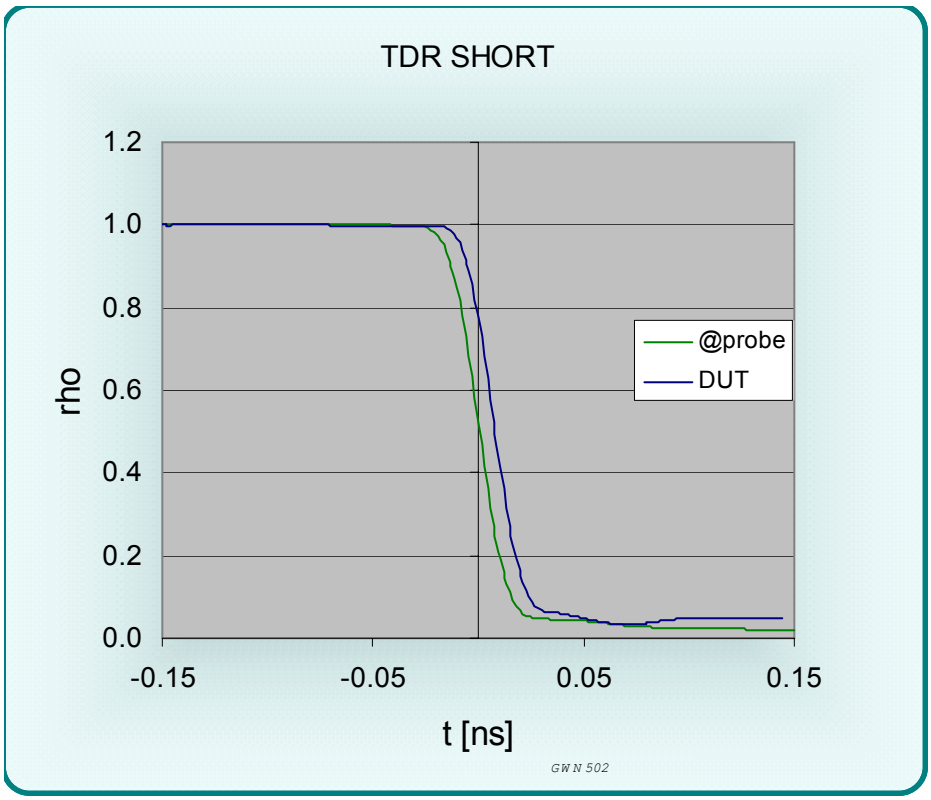


Figure 6 TDR signal from an OPEN circuited — CSP interconnect

For the short circuited CSP interconnect the fall time is about 27.0 ps. This is again no increase over the system risetime of 27.0 ps.

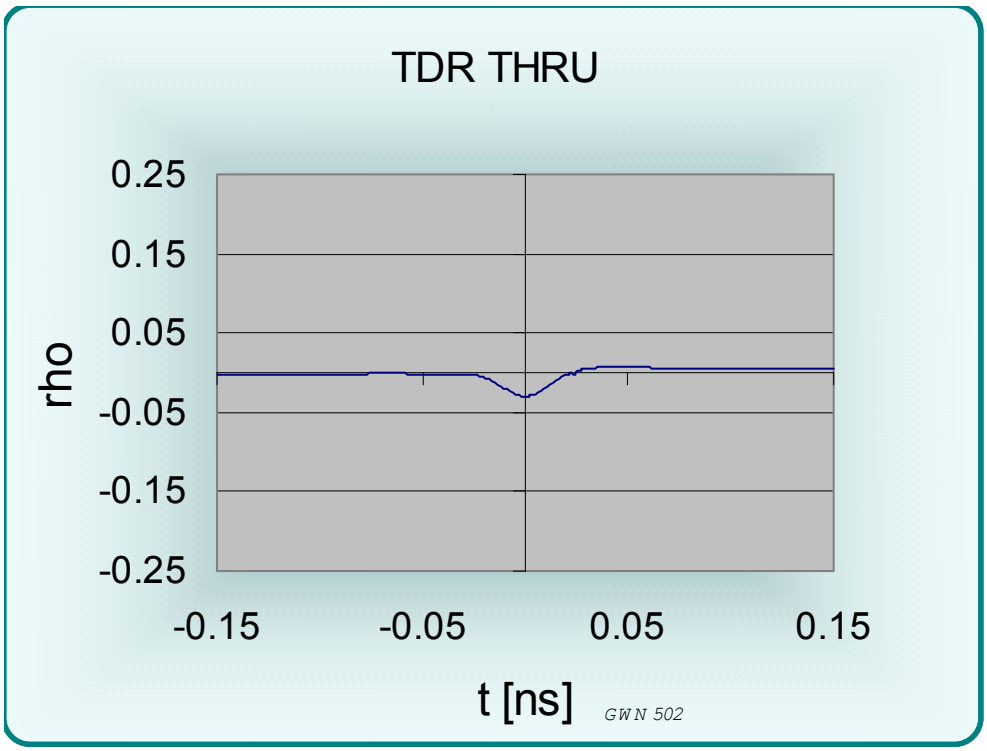


Figure 7 TDR measurement into a 50 Ohm probe

The thru TDR response shows a slightly capacitive response. The peak corresponds to a transmission line impedance of 50.7 Ohms, the dip to 47.1 Ohms. The dip is possibly caused by fixture pad's presence to the socket material, which causes capacitive loading.

The TDT performance for a step propagating through the pin arrangement was also recorded:

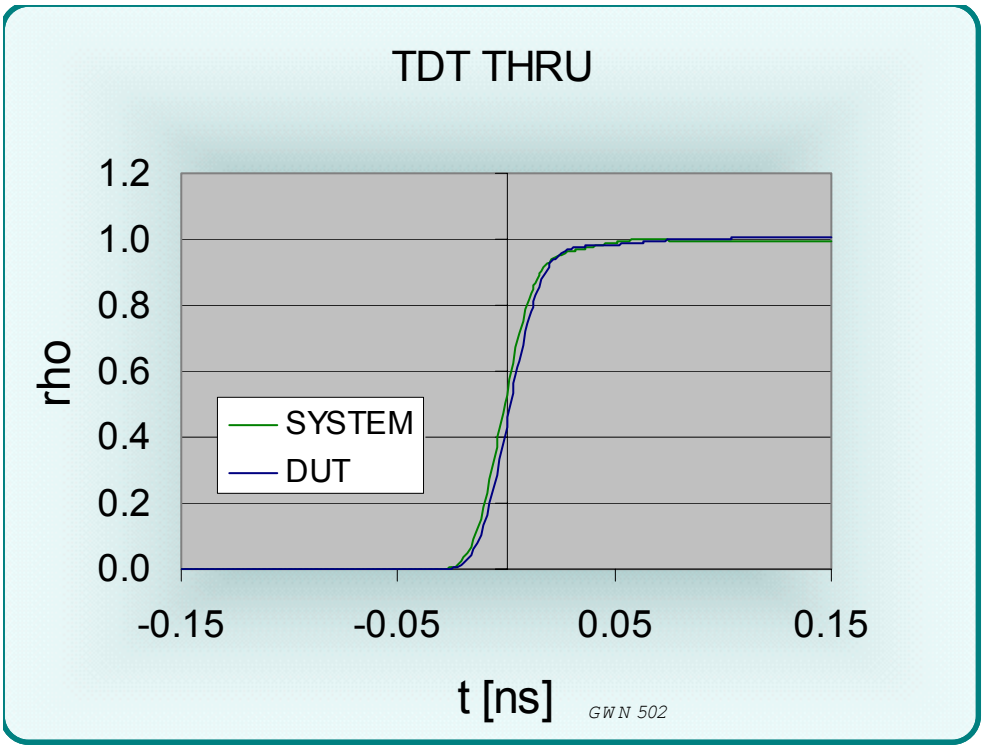


Figure 8 TDT measurement

The TDT measurements for transmission shows no contribution to risetime from the socket (10-90% RT = 30.0 ps, the system risetime is 30.0 ps). The added delay at the 50% point is 2.5 ps. There is no significant signal distortion. If the 20%-80% values are extracted, the risetime is 19.5 ps vs. 19.5 ps system risetime.

**Frequency domain**

Network analyzer reflection measurements for a single sided drive of the signal pin with all other pins open circuited at the opposite end were performed to determine the pin capacitance. The analyzer was calibrated to the end of the probe and the phase of S11 was measured. From the curve the capacitance of the signal contact to ground can be determined (see Fig. 10).

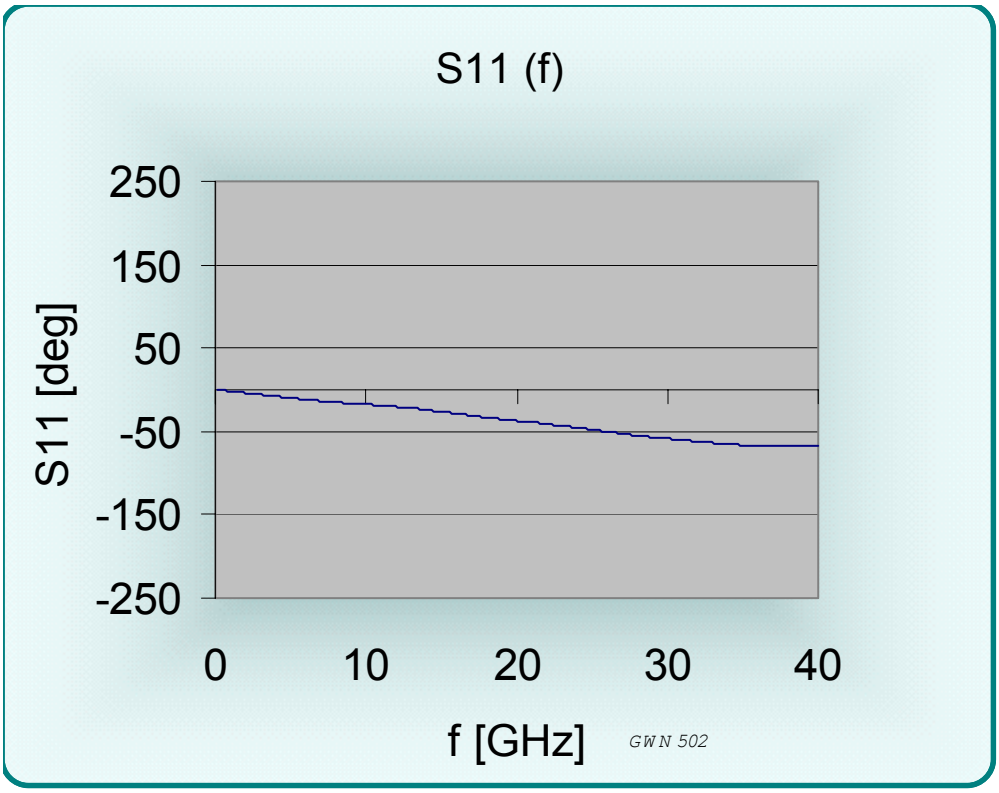


Figure 9 S11 phase (f) for the open circuited signal pin

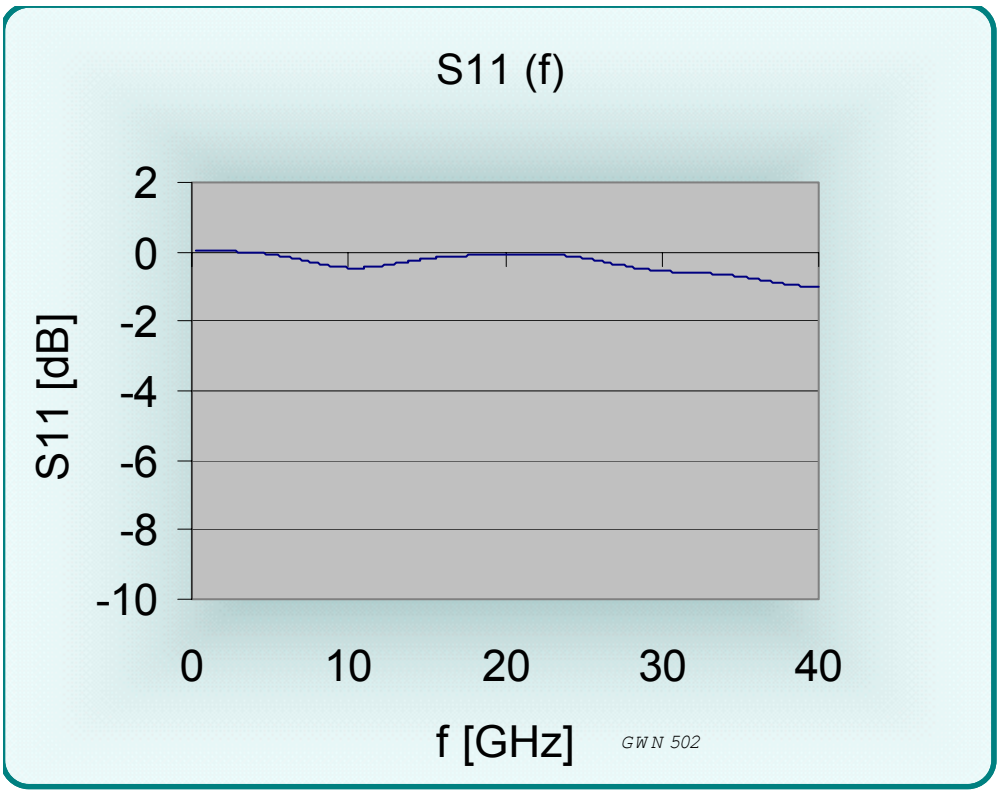


Figure 10 S11 magnitude (f) for the open circuited signal pin

While ideally the magnitude of S11 should be unity (0 dB), loss, radiation and resonances in the array are likely contributors to noticeable return loss for the open circuited pins at elevated frequencies.

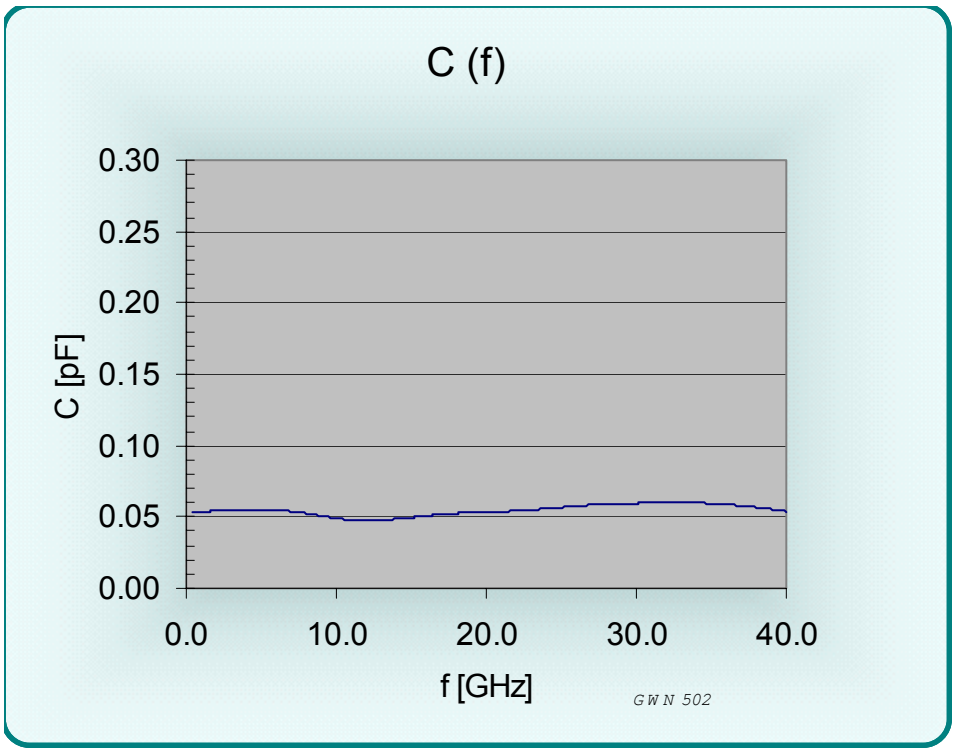


Figure 11 C(f) for the open circuited signal pin

Capacitance is 0.05 pF.

The Smith chart measurement for the open circuit shows no resonances toward the upper frequency limit of 40 GHz. Only a small loss term is present.

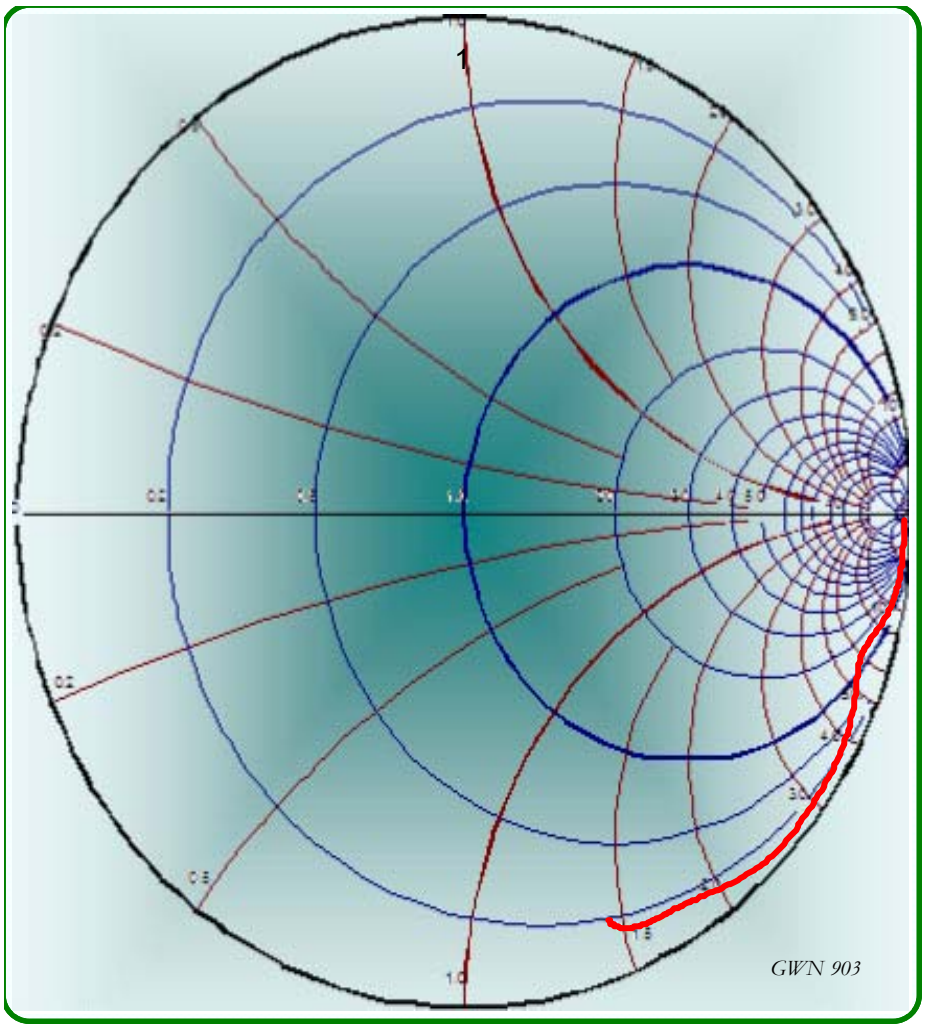


Figure 12 Reflections from the open circuited CSP interconnect

To extract the pin inductance, the same types of measurements were performed with a shorted pin array. Shown below is the change in reflections from the CSP interconnect. Calibration was established with a short placed at the end of the coax probe.

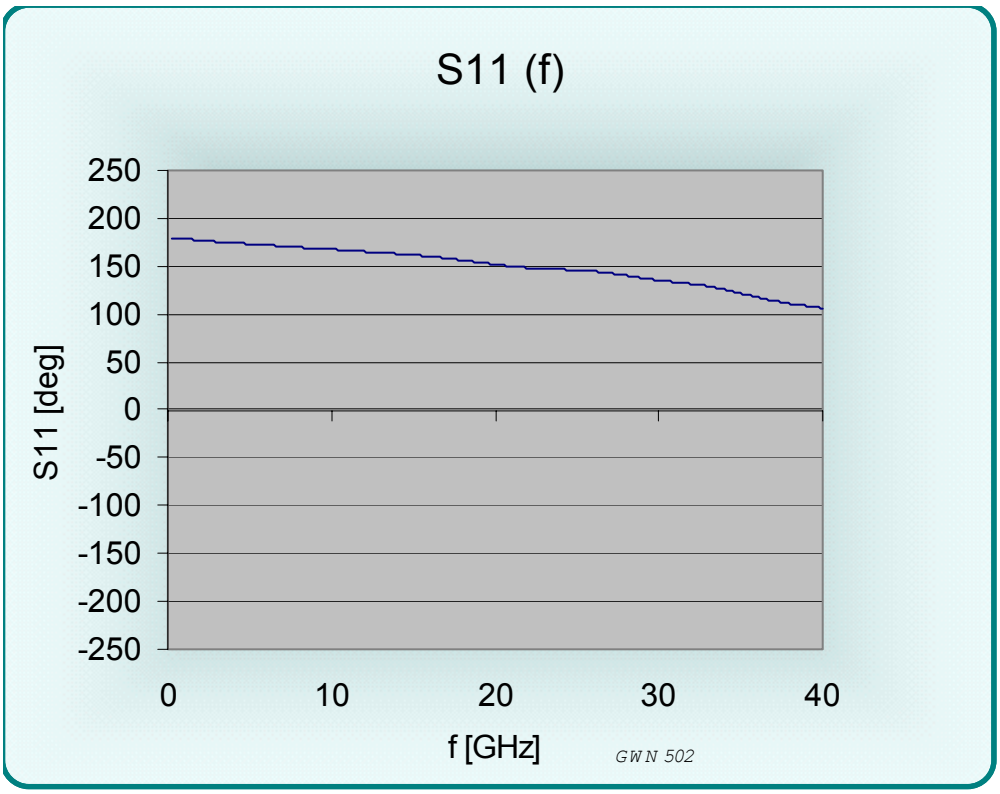


Figure 13 S11 phase (f) for the short circuited case

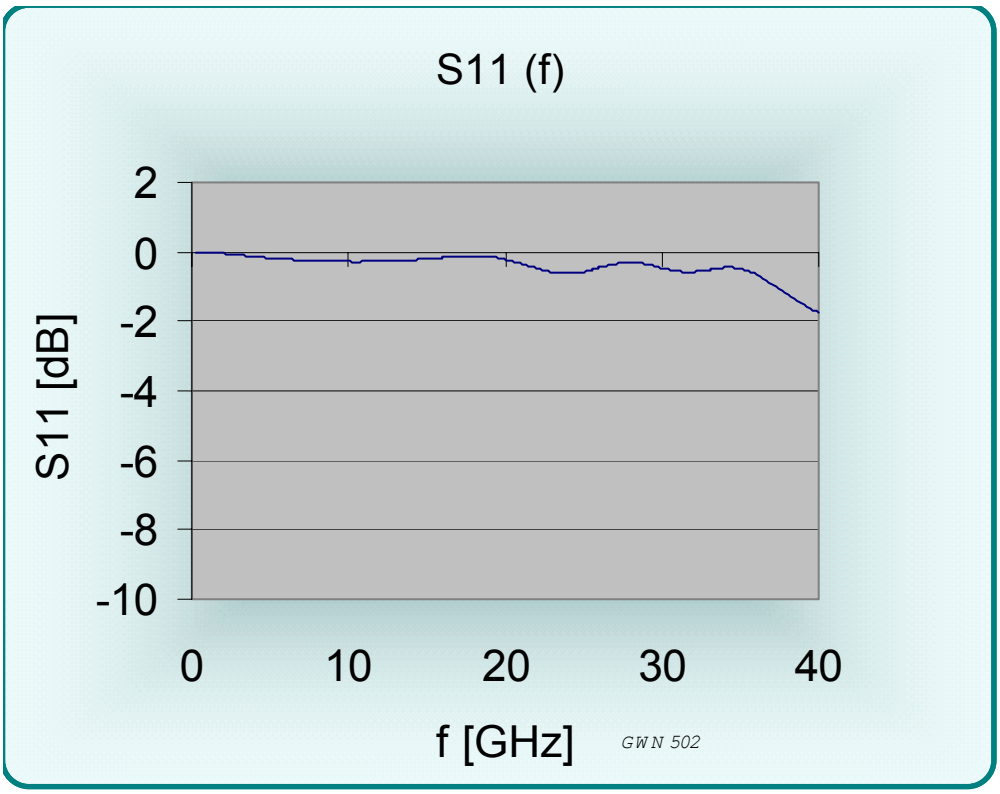


Figure 14 S11 magnitude (f) for the short circuited case

A small loss exists, possibly the result of radiation and dielectric loss and calibration uncertainties.

The phase change corresponds to an inductance of 0.11 nH (see Fig. below).

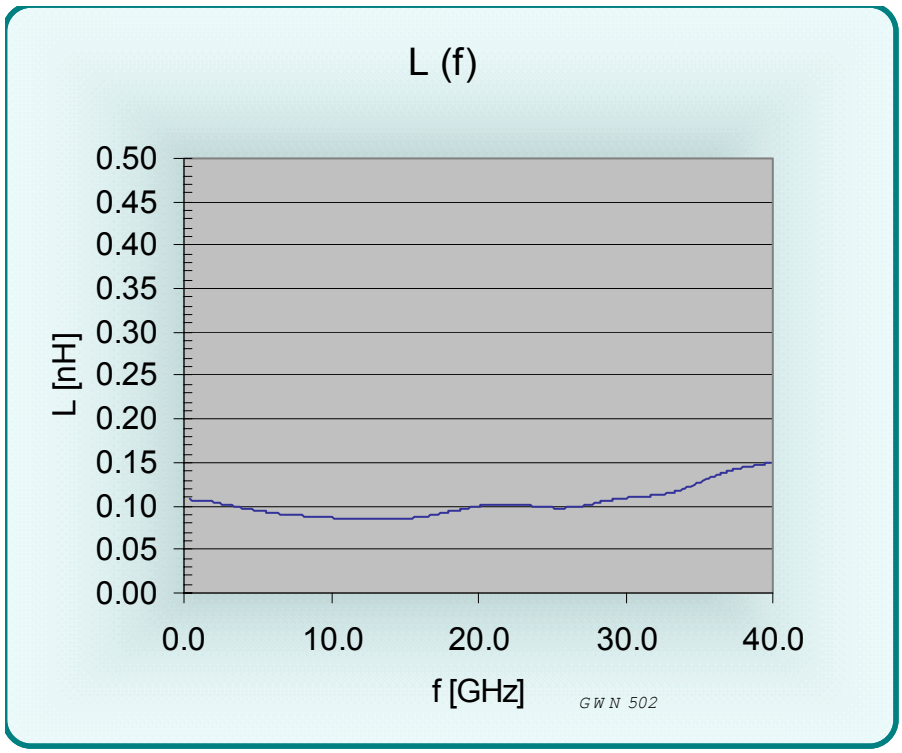


Figure 15 L(f) for the CSP interconnect

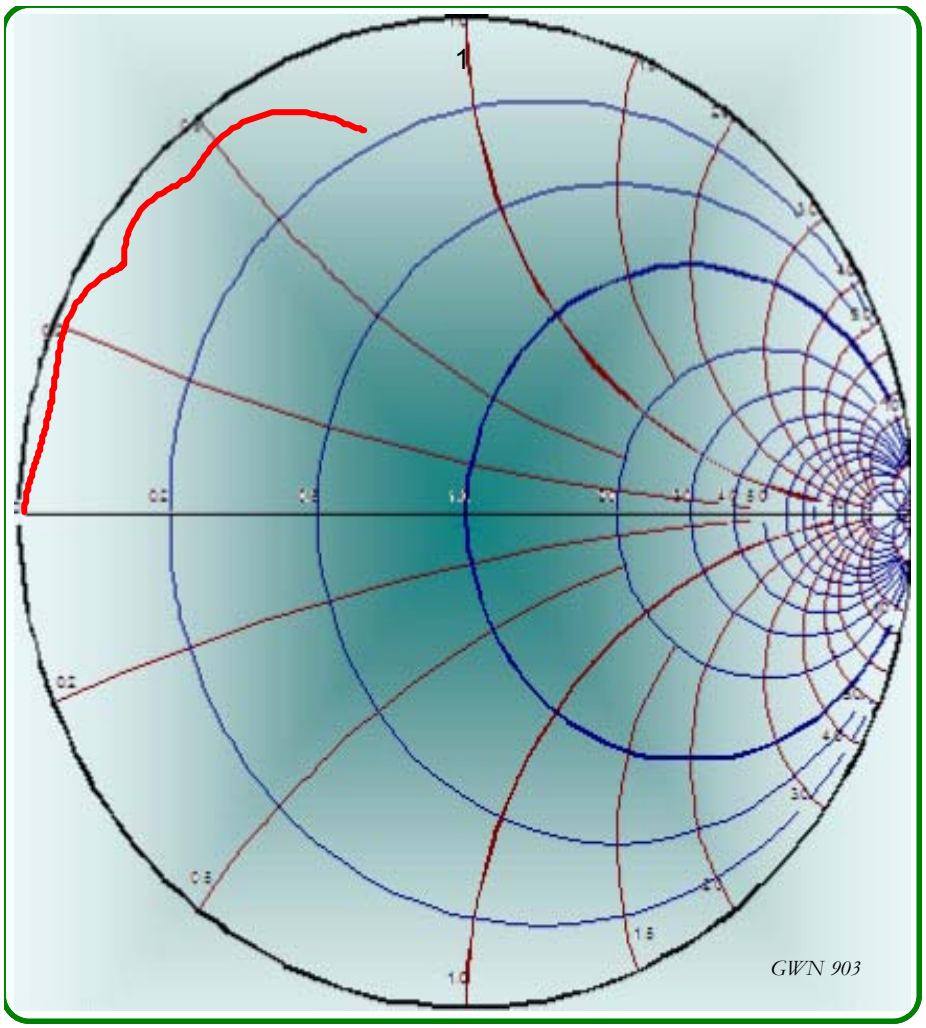


Figure 16  Short circuit response in the Smith chart

Little loss and only  small aberrations are noticeable in the Smith chart for the short circuit condition.

An insertion loss measurement is shown below for the frequency range of 50 MHz to 40 GHz.

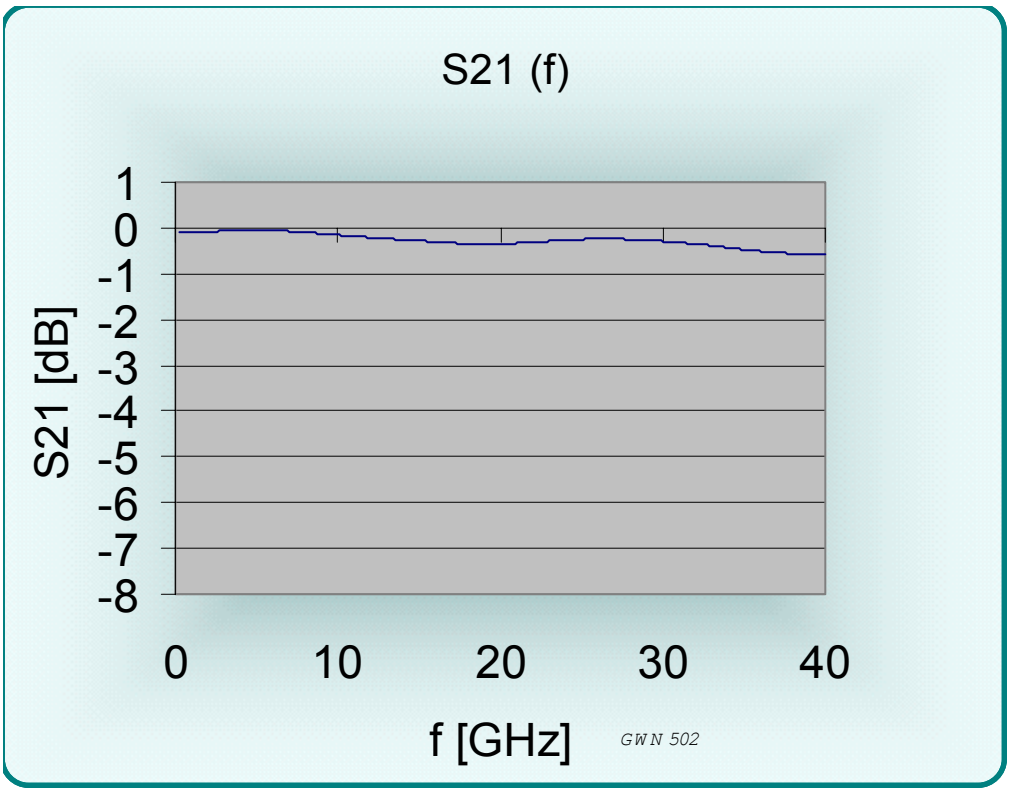


Figure 17 Insertion loss S21 (f)

Insertion loss is less than 1 dB to about 40.0 GHz. The 3 dB point is not reached before 40.0 GHz.

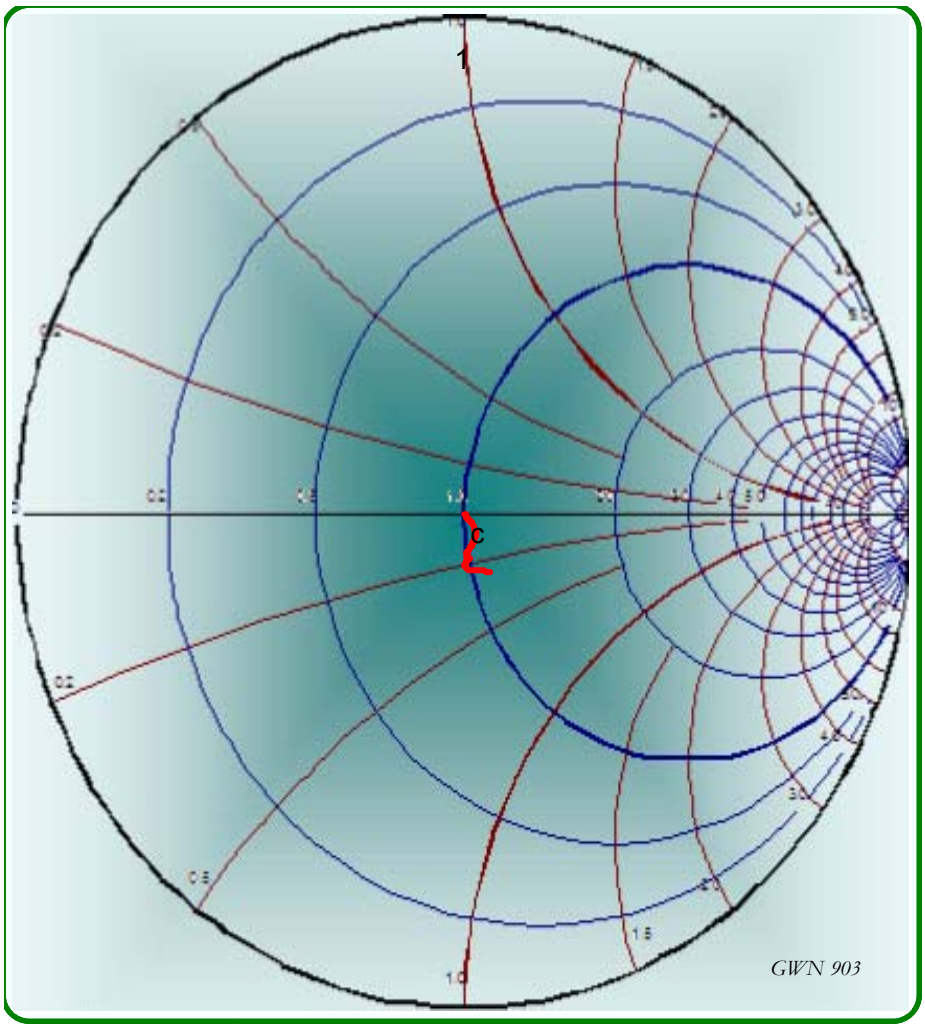


Figure 18  Smith chart for the thru measurement into a 50 Ohm probe

The Smith chart for the thru measurements shows a reasonable match with some reactive components toward 40 GHz.

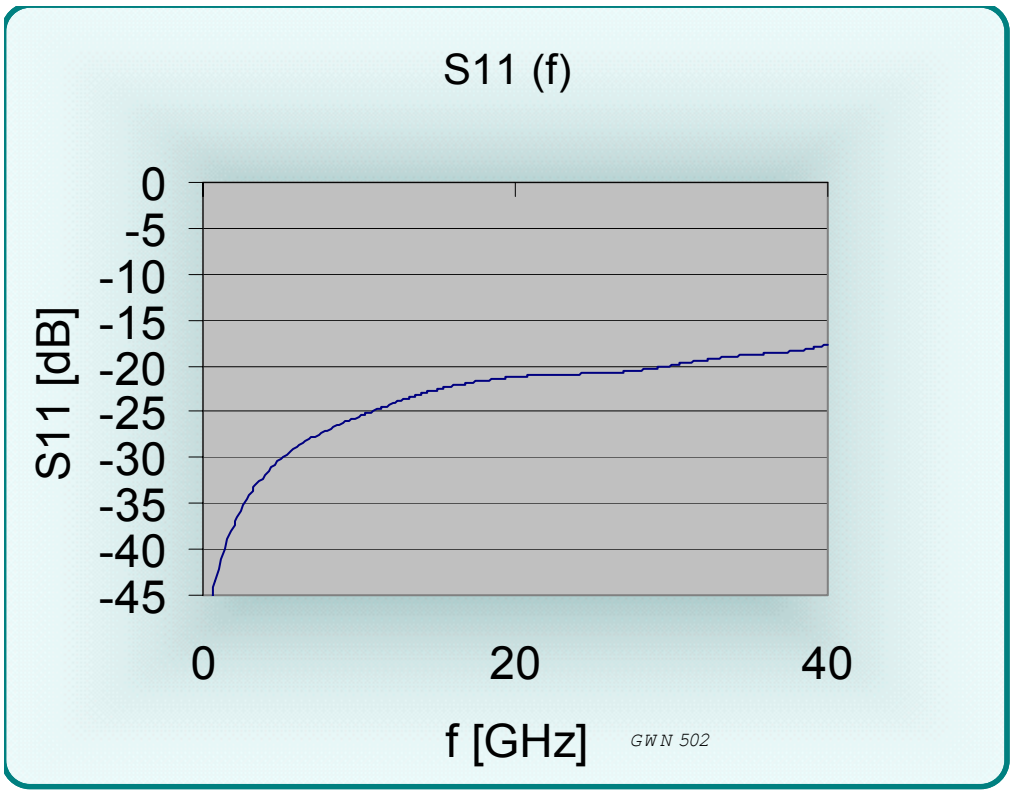


Figure 19 S11 magnitude (f) for the thru measurement into a 50 Ohm probe

Measurement results are near the system limits.

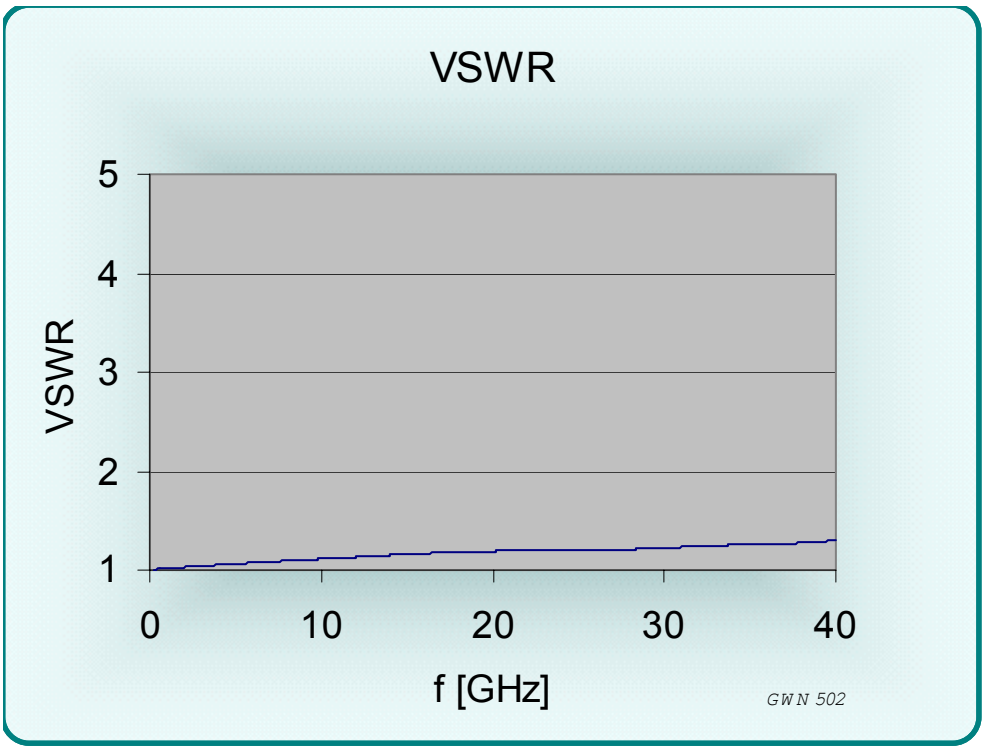


Figure 20  Standing wave ratio VSWR (f) [1 / div.]

The VSWR remains below 2 : 1  to a frequency of 40.0 GHz.

Crosstalk was measured in the G-S-S-G configuration by feeding the signal pin and monitoring the response on an adjacent pin.  Measurement results can be found in the section on the G-S-S-G configuration.

The mutual capacitance and inductance values result from G-S-S-G modeling and are also listed in that section.

## *Measurements G-S-S-G*

### Time domain

Again, the time domain measurements will be presented first. A TDR reflection measurement is shown in Fig. 21 for the thru case at port 1 to port 2:

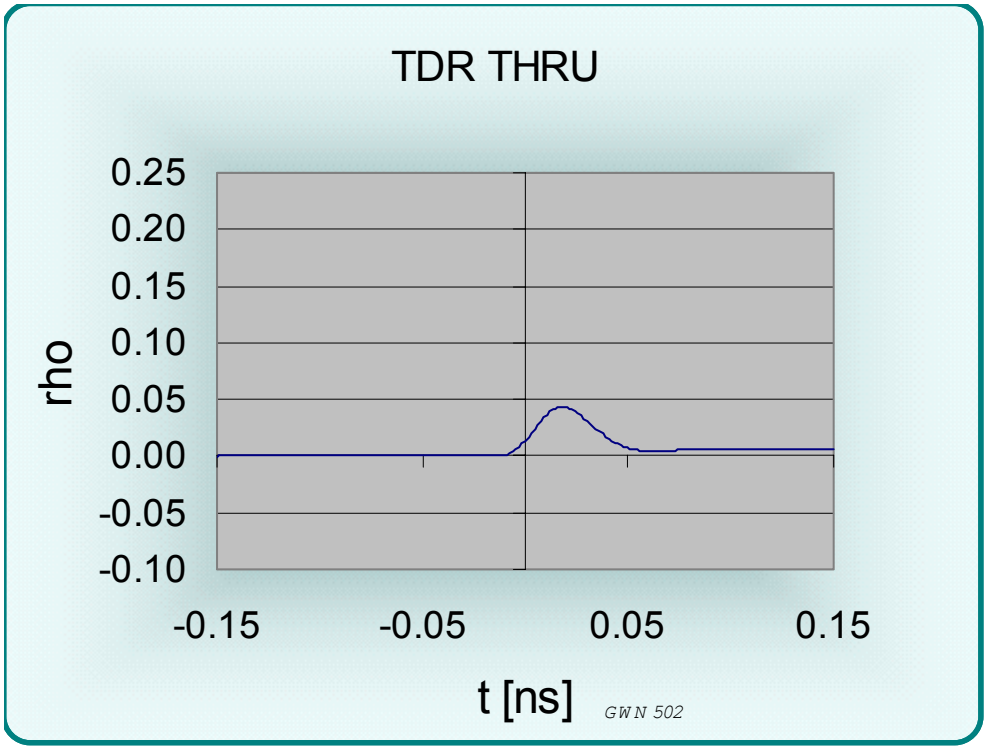


Figure 21 TDR through DUT into a terminated probe

The thru TDR response shows both inductive and capacitive responses. The peak corresponds to a transmission line impedance of 54.5 Ohms. This is higher than in the GSG case, most likely because of the fact that one of the adjacent pins is not grounded.

The TDT performance for a step propagating through the G-S-S-G pin arrangement was also recorded:

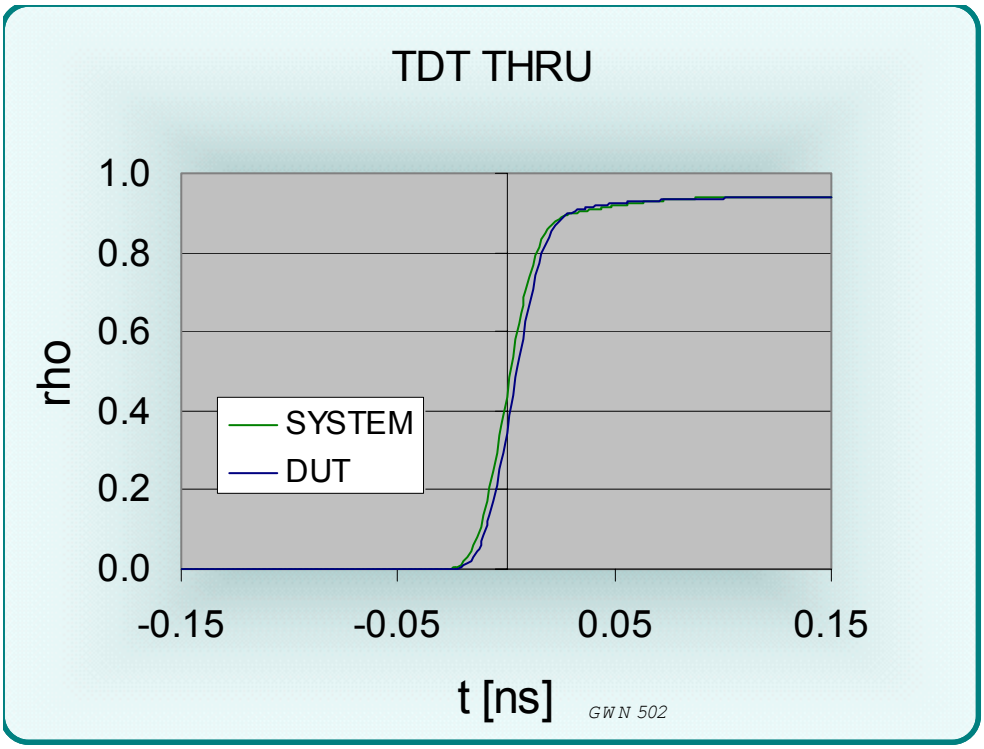


Figure 22 TDT measurement

The TDT measurements for transmission show a noticeable contribution to risetime from the pin array (10-90% RT = 30.0 ps, the system risetime is 30.0 ps). The likely source is the elevated impedance of the pin array. The added delay at the 50% point is 3.0 ps.

**Frequency domain**

Network analyzer reflection measurements for the G-S-S-G case were taken with all except the pins under consideration terminated into 50 Ohms. As a result, the scattering parameters shown below were recorded for reflection and transmission through the contact array.

First, insertion loss measurements (S21 and S12) are shown for port 1 to port 2.

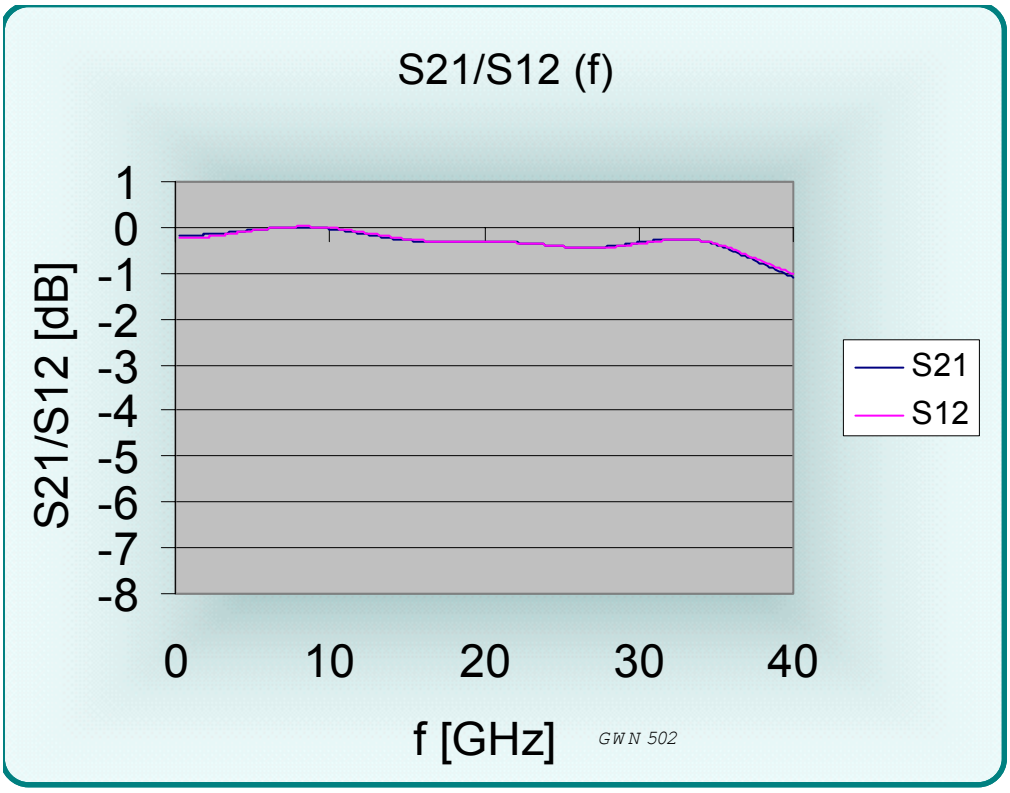


Figure 23 Insertion loss S21 (f) and S12 (f)

Insertion loss is less than 1 dB to about 39.3 GHz and 39.9 GHz for S21 and S12, respectively. The 3 dB point is not reached before 40.0 GHz (S21) and 40.0 GHz (S12).

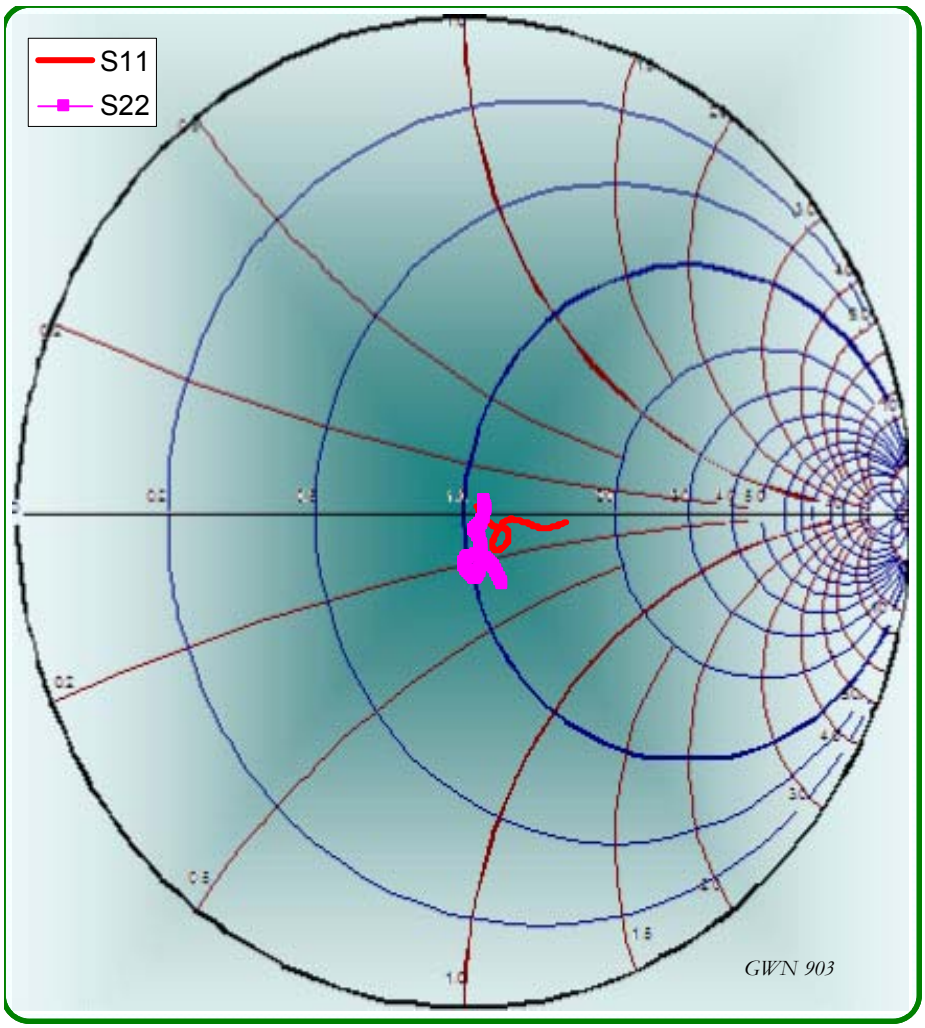


Figure 24  Smith chart for the thru measurement into a 50 Ohm probe

The Smith chart for the thru measurements shows a good match with some reactive components toward 40 GHz.

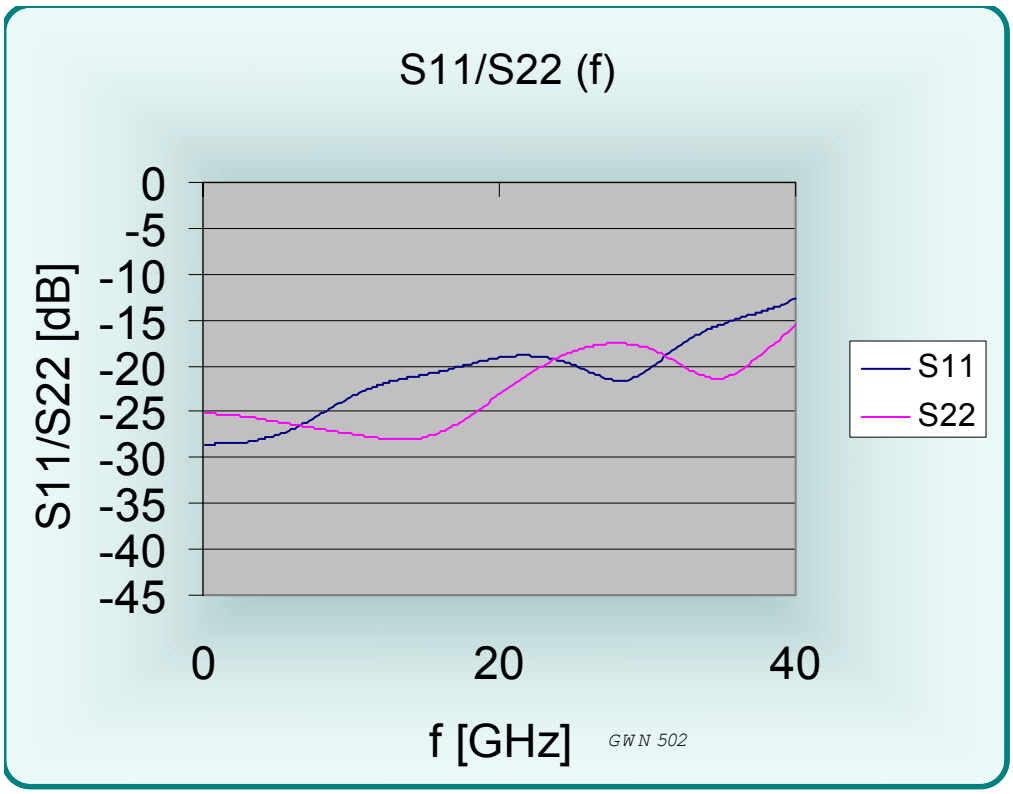


Figure 25 S11 magnitude (f) for the thru measurements into a 50 Ohm probe

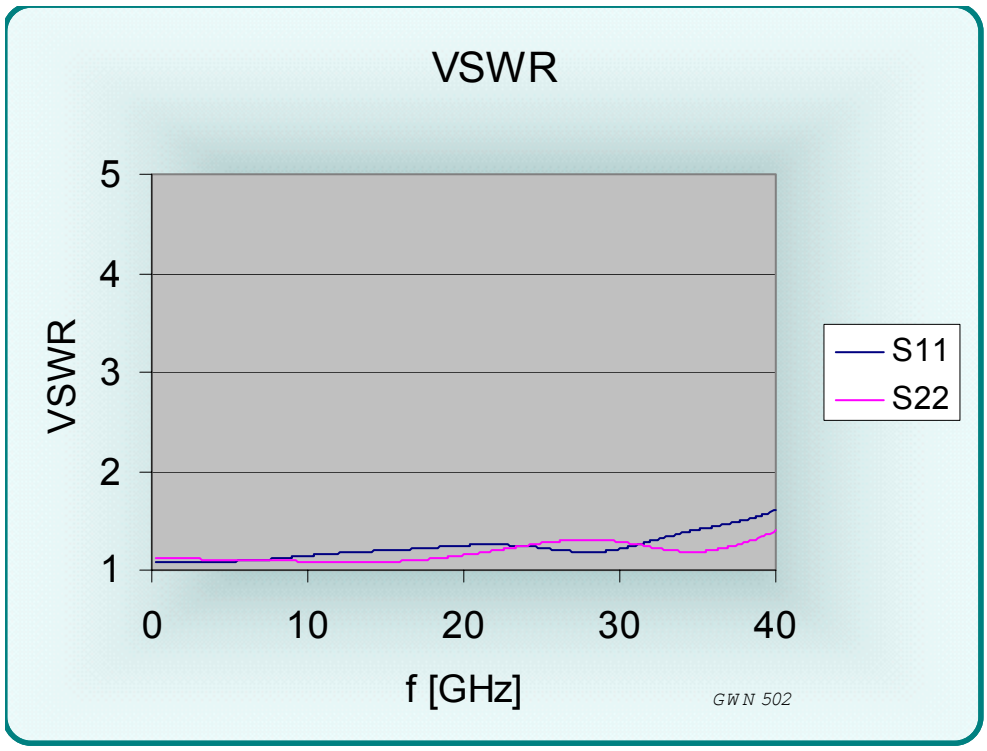


Figure 26  Standing wave ratio VSWR (f) [1 / div.]

The VSWR remains below 2 : 1  to a frequency beyond 40.0 GHz for S11 and 40.0 GHz  for S22.

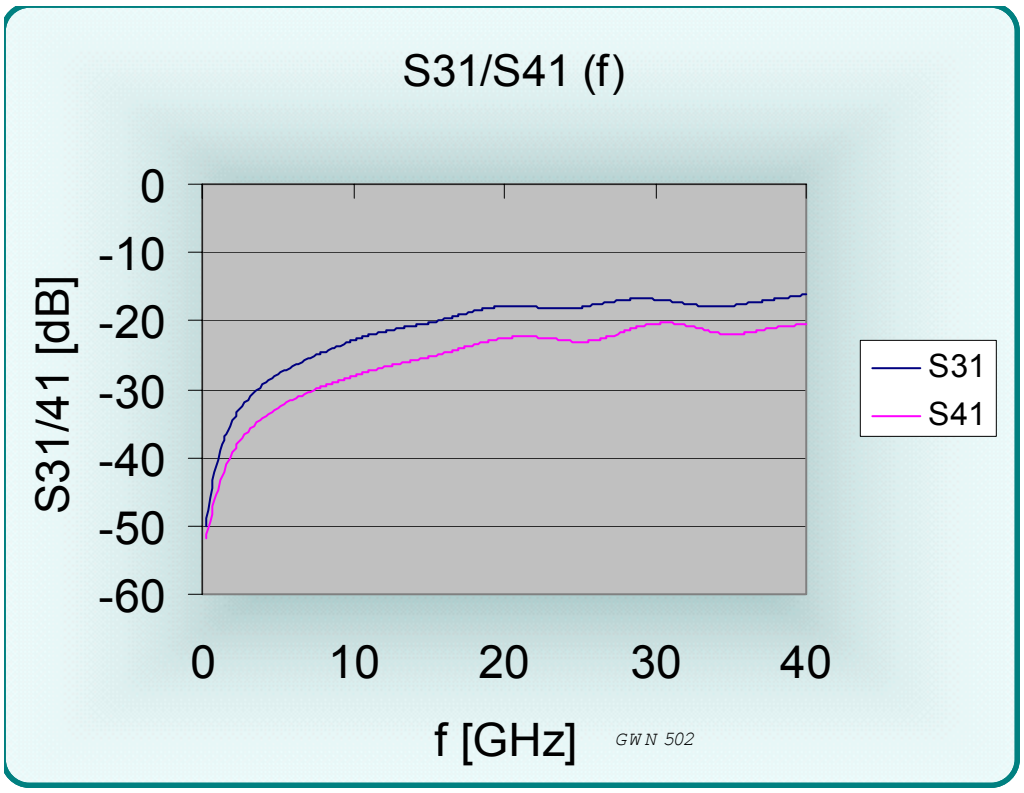


Figure 27 Crosstalk as a function of frequency

The graph shows forward crosstalk from port 1 to port 4 (S41) and backward crosstalk from port 1 to the adjacent terminal (port 3, S31). The -20 dB point is reached at 15.5 GHz (S31) and 40.0 GHz (S41). At 10.2 GHz (S31) and 40.0 GHz (S41) the level of signal reaches -10 dB.

For the purpose of model development the open circuit and short circuit backward crosstalk S31 is also recorded. It is shown below. Model development yields a mutual capacitance of 0.028 pF and a mutual inductance of 0.015 nH.

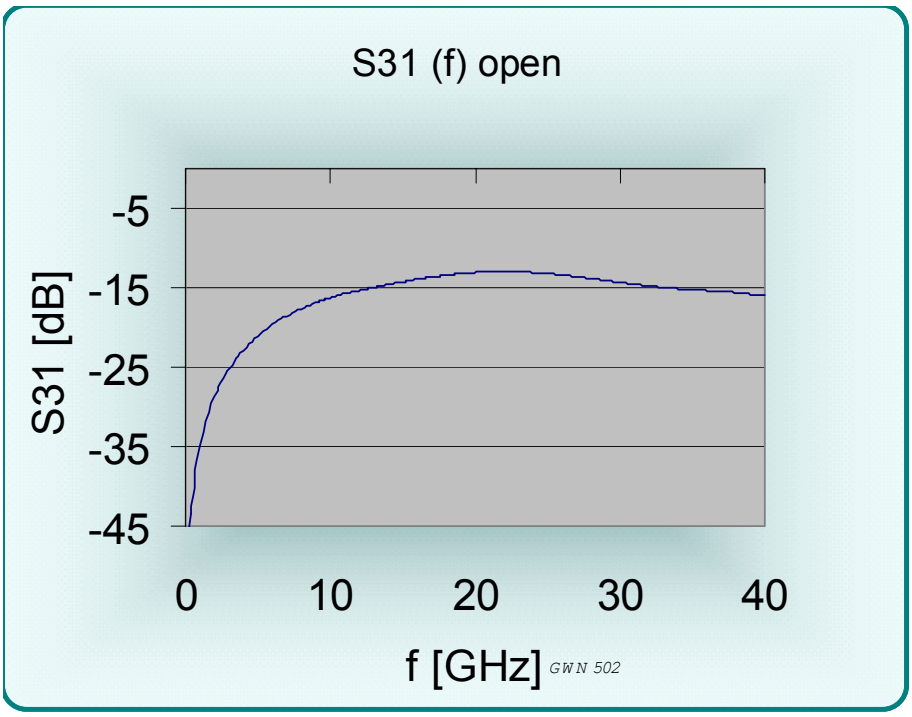


Figure 28 Open circuit crosstalk from port 1 to port 3

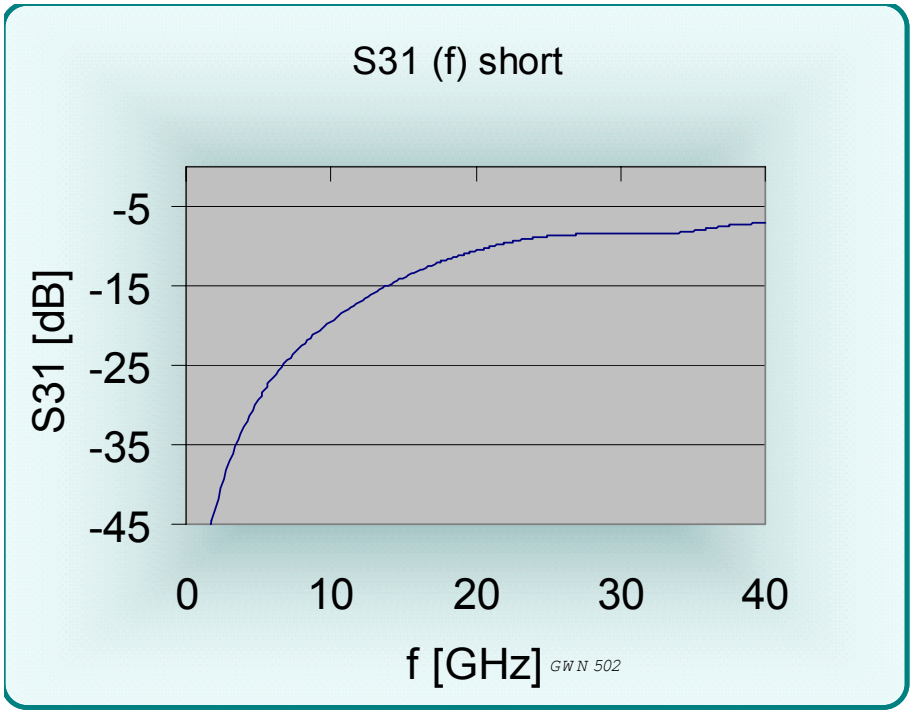


Figure 29 Short circuit crosstalk from port 1 to port 3

## *SPICE Models*

A lumped element SPICE model for the CSP interconnect in G-S-G configuration is shown below:

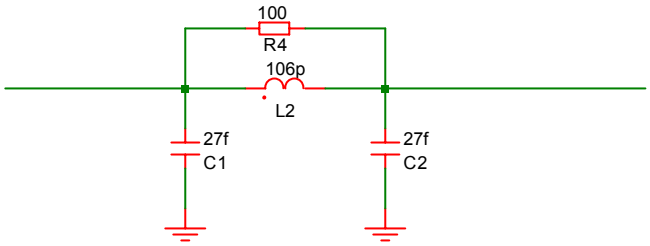


Figure 30 Lumped element SPICE model

The resistor R4 models the loss term. Toward the cutoff frequency of the Pi section the lumped element model becomes invalid. This, however, does not happen before 40 GHz for the above model because of the short socket electrical length. For completeness, the second model developed is a transmission line model:


Figure 31 Transmission line model for the CSP interconnect

The array configuration with signal connections surrounded by ground connections provides a transmission line environment.

**Time domain**

The TDR simulation results indicate an inductive response just as the measurement (Fig. 5, TDR THRU).

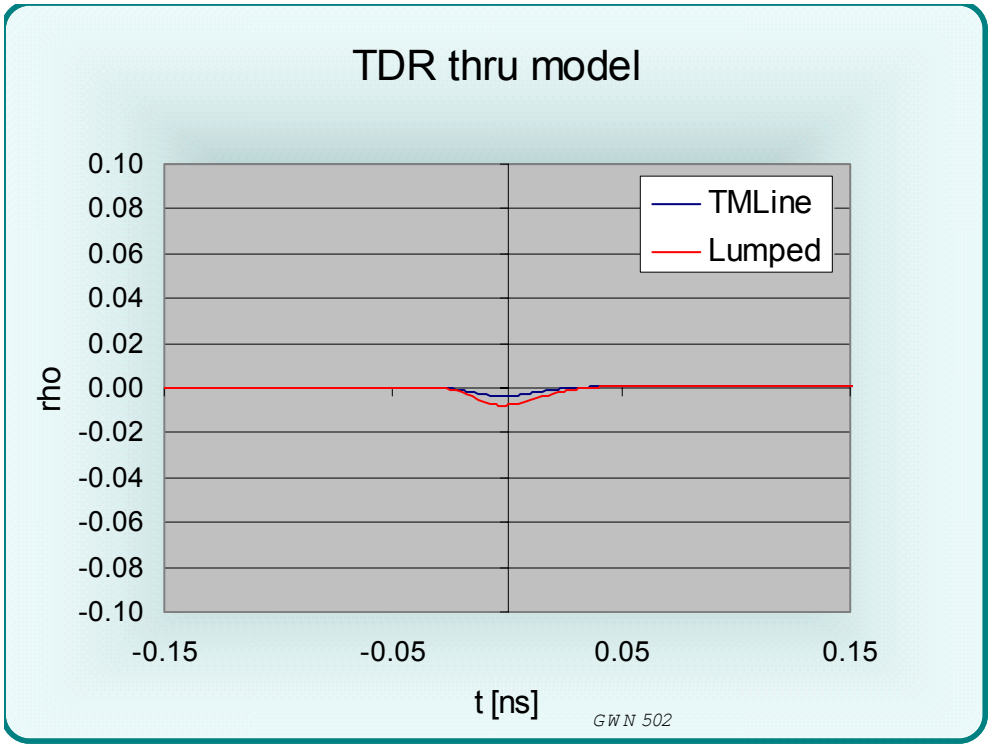


Figure 32 TDR model results

Differences between the two models are small since impedance of the socket is very close to 50 Ohms and the electrical socket length is very short.

The risetime contribution of a signal transmitted through the pin is shown below:

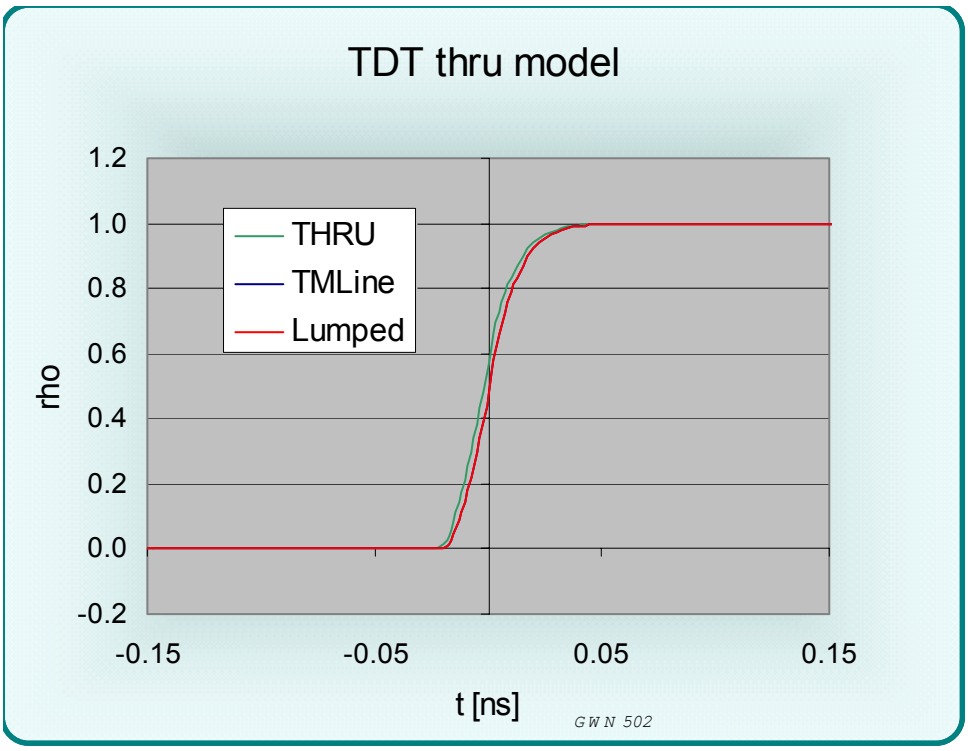


Figure 33 TDT model

The risetime for the transmission line case is 27.5 ps and 27.5 ps for the generator in the model. The lumped element model risetime is also 27.5 ps. This is comparable to the measurement (Fig. 6).

**Frequency domain**

The model's phase responses are also divided into lumped element and transmission line equivalent circuits.

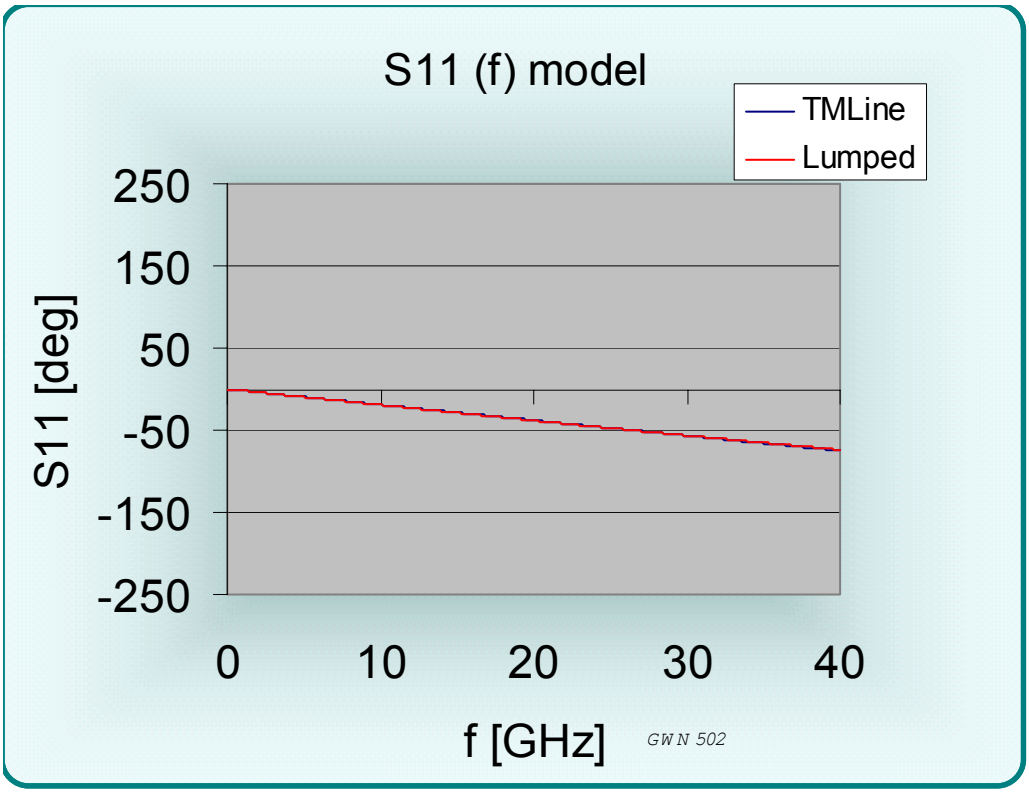


Figure 34 S11 phase (f) for open circuited case

The evolution of phase with frequency is comparable to that measured. Aberrations are likely absent because the measurement contains effects of array resonances and small impedance mismatches that are not completely removed by the error correction process.

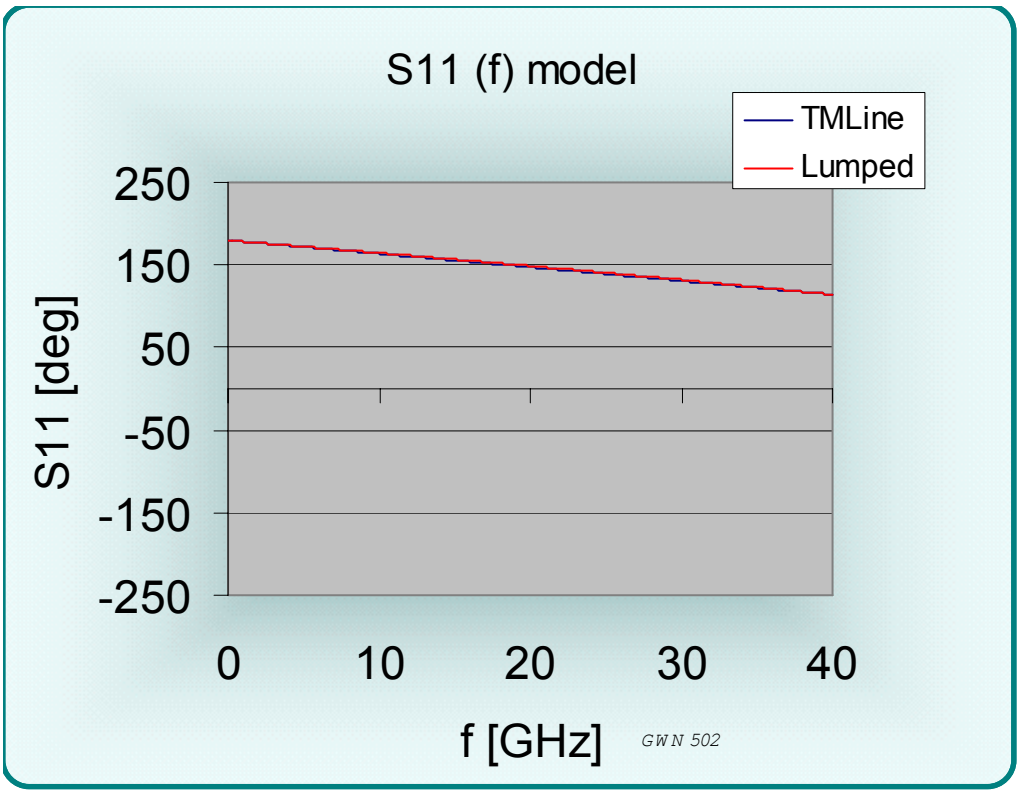


Figure 35 S11 phase response (short circuit)

The short circuit phase evolution with frequency is also comparable to that actually measured.

The insertion loss results below also clearly demonstrate the limits of the lumped element model. As the frequency approaches the cutoff frequency for the Pi section, the insertion loss increases significantly. The transmission line model does not suffer from this shortcoming. It does not, however, account completely for the actual response since coupling to adjacent pins is absent in this model.

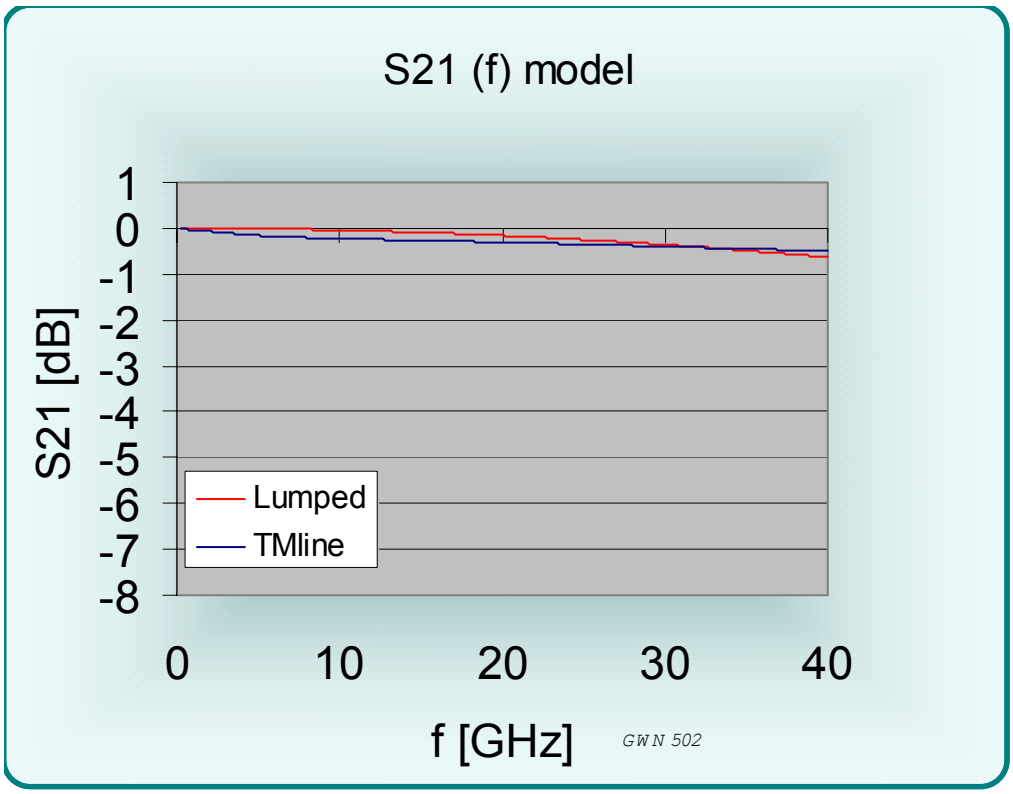


Figure 36 Insertion loss as a function of frequency

The lumped element frequency domain model used for evaluating the mutual elements also consists of the three sections of the single pin plus a mutual inductance and two coupling capacitors. The model was used in configurations corresponding to the actual measurements.

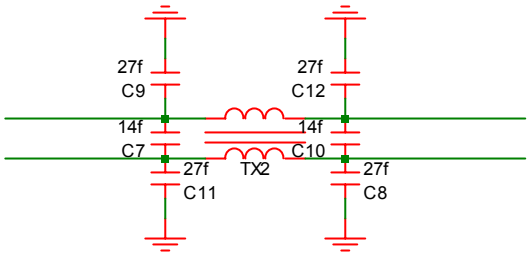


Figure 37 Equivalent circuit for mutual coupling

A transmission line model with coupled transmission lines and added loss terms was also established:

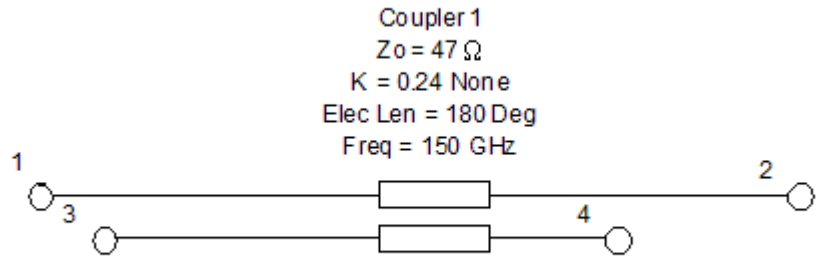


Figure 38 Transmission line equivalent circuit for crosstalk

The model shows a coupled transmission lines with the respective in- and outputs.

When comparing the results with the measurements it is apparent that the lumped model produces more favorable results for the forward crosstalk than the transmission line model, while both models are representing the backward crosstalk well. No explanation for the discrepancy has been found.

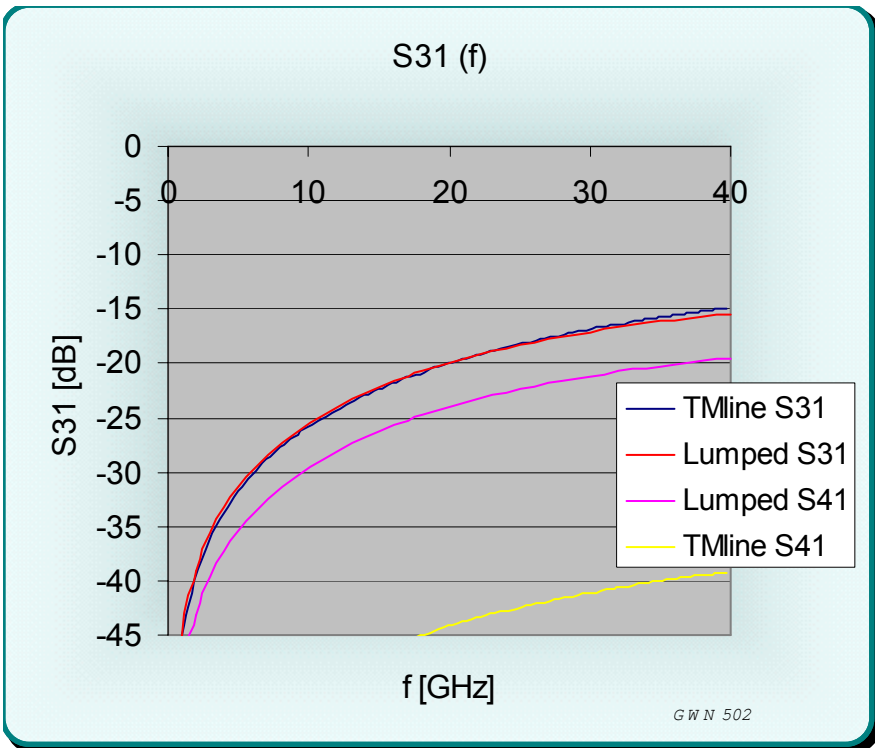


Figure 39 Crosstalk S31 and S41 [dB] as a function of frequency

CSP Interconnect

Report summary sheet

10/26/04

## *Socket test configuration:*

All pins grounded in an 0.5 mm pitch array except for one signal pin ( G-S-G ) and two signal pins in the G-S-S-G configuration.

## *Performance:*

**Time domain:**

| | | | |
|---|---|---|---|
| Signal delay | | = | 2.5 ps |
| Risetime, open circuit | | < | 28.5 ps |
| Risetime, short circuit | | < | 27.0 ps |
| Risetime, thru 50 Ω | | < | 30.0 ps |

**Frequency domain:**

| | | |
|---|---|---|
| Insertion loss | < | 1 dB to 40.0 |
| VSWR | < | 2 :1 to 40.0 |

**Equivalent circuit parameters:**

| | | |
|---|---|---|
| Pin inductance | = | 0.11 nH |
| Pin to ground capacitance | = | 0.05 pF |
| Mutual inductance | = | 0.015 nH |
| Mutual capacitance | = | 0.028 pF |
| Transmission line | = | Z0 = 47.1 Ω , Tl 2.3 ps |