

Enhanced interconnect medium simplifies test & verification

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Abstract

In high performance embedded systems test application, the requirement for accurate measurement of AC and DC parameter is often critical. During development phase, IC devices are not permanently attached to the target board. Instead IC devices are connected via interconnect medium to the target board. The spring probe is one of the typical interconnect medium. Spring probes have to be compressed to certain height for making reliable electrical connection. Since the IC devices are not perfectly planar, each of the spring probes can be compressed to different height which causes variation in the electrical resistance for each signal path [3]. This variation causes signal transmission to fail sometimes and the process needs to be repeated by re-seating the IC device. This paper will discuss a new feature added to the spring probe providing electrical resistance within 2-3 milliohms irrespective of the compression height. This enhanced feature allows system developers to test & verify without multiple intervention. Presentation will specifically address electrical resistance over multiple cycles and other high performance characteristics of the interconnect medium.

Introduction

As more functionality is included in integrated circuits, there is an increasing need to make extremely accurate voltage measurements or force extremely accurate voltages to perform DC parameter tests and measure AC characteristics as well. The only way that these tests can be performed accurately and repeatedly in a test environment, over many insertions, is to contact the device through an interconnect medium whose contact resistance variation is less than a few milliohms. For example, an increasingly common DC parameter test is RDSON – the resistance between drain and source when a FET is turned on [1]. This parameter can be as little as a few milliohms. Attempting to measure this parameter through spring probes that is nominally tens to hundreds of milliohms and can vary in tens of milliohms from insertion to insertion is not practical. Alternatively, Kelvin connection eliminates contact resistance as an issue by making a separate force and sense contact to the target device pad. Kelvin connection requires two spring probes to contact the same device pad. This brings additional mechanical alignment challenges. Still AC tests such as communication to ports or other external module depend on spring probe interconnectivity.

Spring Probe Contact Resistance

To determine the contact resistance of spring probe, we need to understand the internal mechanics of spring probe as well as the resistance network that allows the flow of current shown in Figure 1. Double ended spring probes are primarily comprised of two plungers (bottom and top), barrel and spring. The spring (gold plated music wire) is sandwiched between two plungers (gold plated hardened Beryllium Copper) inside the barrel (gold plated Phosphor Bronze) [2]. When assembled, the bottom plunger is compressed to operating height. This will accommodate standard pad height variations on the target PCB. Similarly on the top side, the device compresses top plunger to its operating height to accommodate co-planarity of device. At this condition, the tip of plungers inside the barrel (both top and bottom) will engage with the barrel wall which will allow the flow of current through the cylindrical barrel. Because the device has wide co-planarity, not all the spring probes are compressed exactly to its operating height. If the plungers were not compressed to its operating height, the engagement to barrel wall will be different which in turn results in tens of milliohms variation.

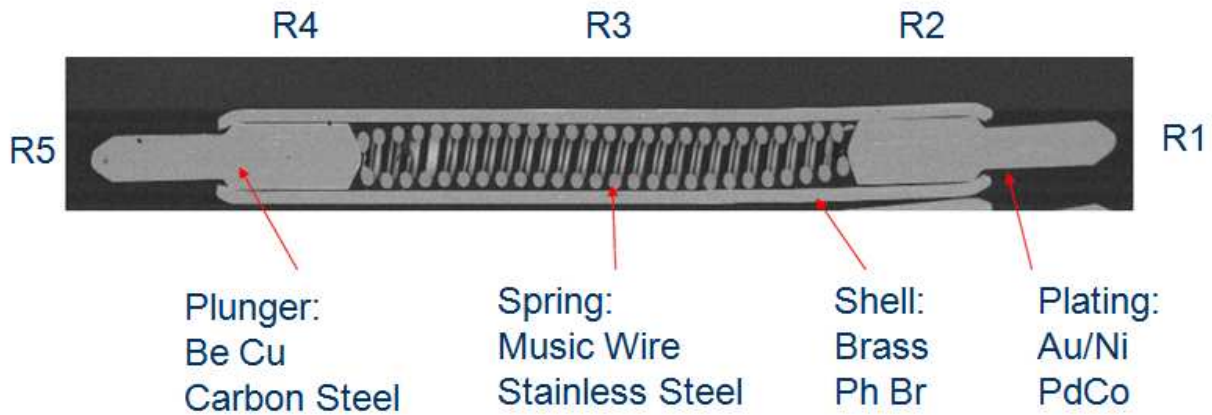


Figure 1: Spring probe internal structure showing material details and resistance network

In Figure 1, R1 represents constriction resistance between device lead and plunger tip. R2 represents constriction resistance between top plunger and inside wall of barrel. R4 represents constriction resistance between bottom plunger and inside wall of barrel. R5 represents constriction resistance between PCB pad and plunger tip. R3 represents total bulk resistance of top plunger, bottom plunger and barrel. Total resistance is $R1+R2+R3+R4+R5$. In this current path, majority of resistance variation is attributed to R2 and R4. When the inside spring compresses to certain distance, a force is applied to the plunger engaging on barrel inside wall. Variation in the compression distance causes variation in the force ultimately resulting in resistance variation.

New Spring Probe Design

The biggest challenge is to eliminate contact resistance variation due to compression height variation. The design shown in Figure 2 eliminates one of the constriction resistance in the network and controls the other using both external compression spring and internal leaf spring. The current flows from solid top plunger to solid bottom plunger eliminating the cylindrical barrel in the new stamped probe design. The new design uses a pinch mechanism that slides in a controlled groove path between the two solid plungers. This pinch mechanism maintains continuity between moving components at all time and at different compression heights.

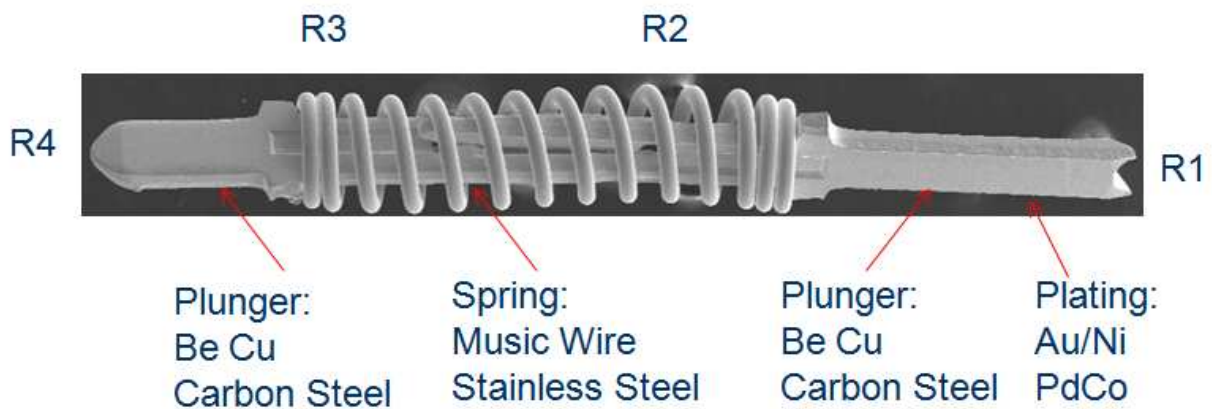


Figure 2: Stamped probe internal structure showing material details and resistance network

R2, R4 in double ended spring probe is replaced by only one resistance component R2 in the new stamped probe design. R2 values are further controlled by pinch mechanism. The disadvantage to this option is that pinch mechanism wears out after multiple back and forth riding in the groove. The pinch tip geometry can be optimized for certain number of cycles which is sufficient enough for semiconductor test and verification of IC devices.

Experimental Setup

To verify the new stamped probe design works better than the existing spring probe design, we conducted few experiments comparing both designs side-by-side in a same experimental set up. Spring probe was referred as SS and the new stamped probe was referred as SBT.

Force-Deflection-Resistance

The first test examines the relationship between deflection of the spring probe, force and the contact resistance. Displacement – Force (DF) test station was used to measure the spring probe deflection and its corresponding force. Spring probes (quantity 36) were assembled into a test fixture. The test fixture with pins was mounted on a board which is connected to a tester for contact resistance measurements. The return electrical path was connected to the force gauge plunger. Test was initialized by moving the force gauge plunger to the tip of the spring probe. Then, force gauge plunger was moved down in increments of 0.01mm and the corresponding force and contact resistance were recorded. The test was repeated for all the 36 spring probes. The whole set up was repeated for new stamped probe. Averages and standard deviations were calculated. Figure 3 shows the force versus deflection curve for both SS and SBT pins. It can be seen from the graph that the force increases as the displacement increases.

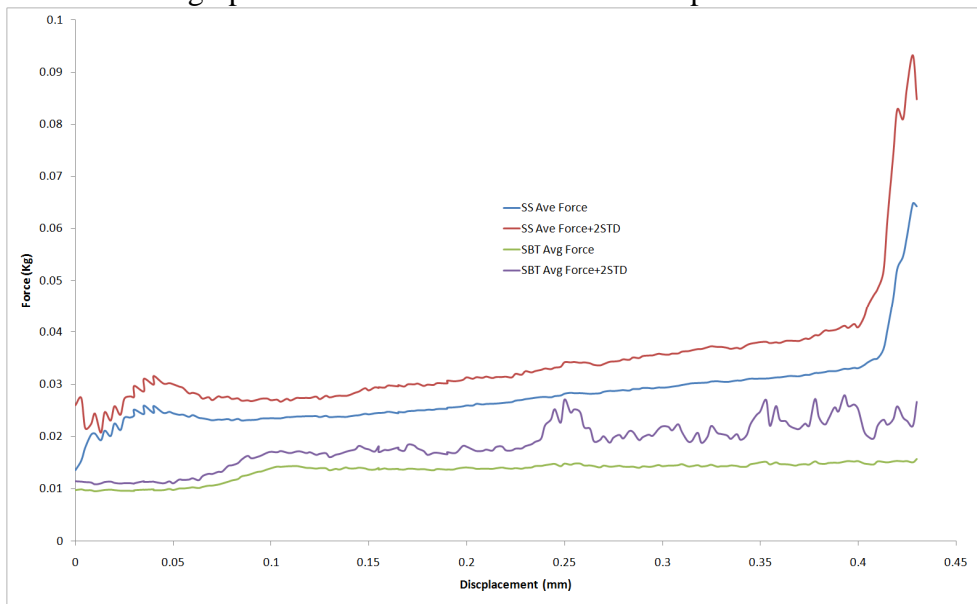


Figure 3: Force versus deflection curves for SS pin and SBT pin

For the SS pin, the average plus two standard deviation force curve was smooth which reflects the internal spring rate. For the SBT pin, the average plus two standard deviation force curve was varying widely. This is due to combination of external compression spring and internal leaf spring. This also makes flat average force curve because one spring compensates for the other. This feature is very important for a socket. When the device is compressed on the pins, we are

concerned with total average force as opposed to individual force. Since the average force is mostly flat over the deflection, it provides a very smooth user operation mode.

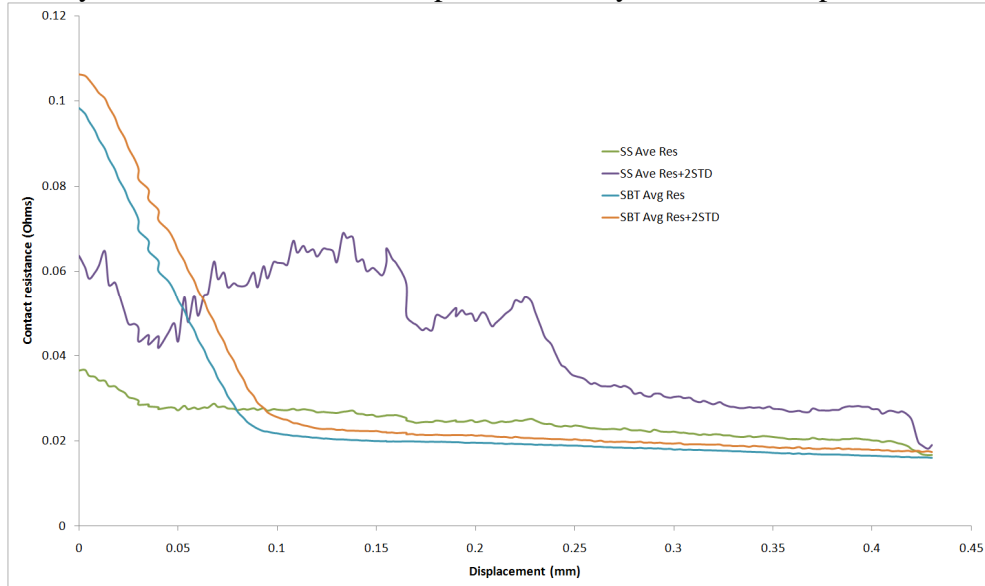


Figure 4: Resistance versus deflection curves for SS pin and SBT pin

On the contrary to the force, contact resistance decreases as the displacement increases as shown in Figure 4. For the SS pin, the average plus two standard deviation resistance curve was varying drastically. This creates major problems in applications. Since the IC devices are not perfectly planar, each of the spring probes compressed to different height which causes variation in the electrical resistance for each signal path. This variation causes signal transmission to fail sometimes and the test process needs to be repeated by re-seating the IC device. For the SBT pin, the average plus two standard deviation resistance curve was smooth and it is only few milliohms variation from the average curve consistently throughout deflection. A desired displacement range was chosen based on the compliance requirement of each application. For example, the desired displacement range is 0.2mm to 0.3mm. Average contact resistance corresponding to this displacement is 20mOhms when using SBT pin and 30mOhms to 50mOhms fluctuation when using SS pins. This information is very important for the test engineer because specific test sequence will fail due to this fluctuation. Since the SBT pin has consistent contact resistance, it helps avoiding false failures and repeating tests by re-seating devices multiple times. Another important factor to be considered is that SBT pins provide consistent low contact resistance with low force. This means lower overall force applied on the device which is a must due to newer IC devices come with very thin wafers to address the demand of the consumer industry.

Life cycle test

The previous experiment proves consistency in single cycle test. In reality, these spring probes go through multiple thousands of cycles during their life time. The second test examines the relationship between contact resistances over spring probes life cycle count. An actual handler was used for this experiment. 500 pins were assembled onto a test fixture that was mounted on the test board which was connected to a tester. A gold plated shorted device simulator was mounted on the plunger head. The test set up was adjusted such that the head moves down 0.3mm which was the chosen travel for the spring probe. Initial contact resistance data was

measured via tester and the ATE (Automatic Test Equipment) was turned on. This moves the plunger back and forth which in turn cycles the spring probe. A digital counter was inserted into the test setup to measure the cycle count. Contact resistance data was collected at different cycle intervals for SS pins. The test was repeated for SBT pins and data was collected and plotted in Figure 5.

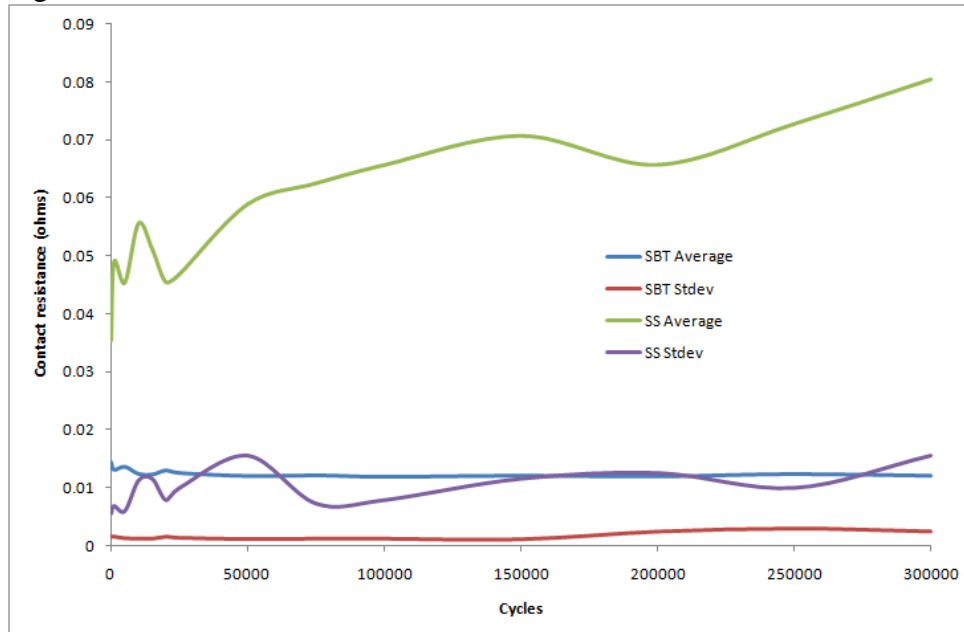


Figure 5: Resistance versus life cycle count for SS pin and SBT pin

It can be seen from the graph that the average contact resistance is less than 15 milli ohms consistently throughout 300,000 cycles. Standard deviation was also shown to provide an understanding of the data spread. Standard deviation for SBT pin is less than 3 milli ohms throughout life cycle. Whereas average contact resistance for SS pins starts at 40 milli ohms and shoots up to 80 milli ohms as the cycle count progresses. Standard deviation for SS pins fluctuates between 5 milli ohms and 15 milli ohms. Based on the graph, it can be concluded that the SBT pin design enables consistency in contact resistance throughout life cycle which in turn enables consistency in the final device test applications.

Current capability test

The current test measures the capability of interconnect medium to carry power without destruction to the system. The SBT pins were assembled inside a test fixture and placed between two metal plates. Au over Ni plating was applied to the surfaces of the brass plates. A four terminal (Kelvin) measurement setup is used that includes a computer controlled voltage source as well as a current source capable of delivering 10 A. The Voltage developed across the contact is recorded in a Kelvin (four terminals) measurement at separate terminals with an HP3456A digital voltmeter. During test, drive current is increased in steps of 50mA to the maximum value. Because of the low thermal mass a fast response of the contact itself occurs. The dwell time for each current step is thus set to 10 seconds. For current handling tests, all pins are isolated except for one. The SBT pin fixture is modified to allow thermocouple access. Current is driven thru the test pin. Once the voltage data is available, it is processed to reveal the resistance and power dissipation as a function of drive current. A second digital meter records the temperature of a small thermocouple (0.010") located near the driven test pin. The thermocouple's access location

is near the center of the pin. Temperature rise is measured via thermocouple in proximity with the pin. This implies that temperature readings at the thermocouple will be lower than those at and inside the pin itself. Since we are comparing between SS and SBT pins, the relative difference in data is critical which is shown in Figure 6.

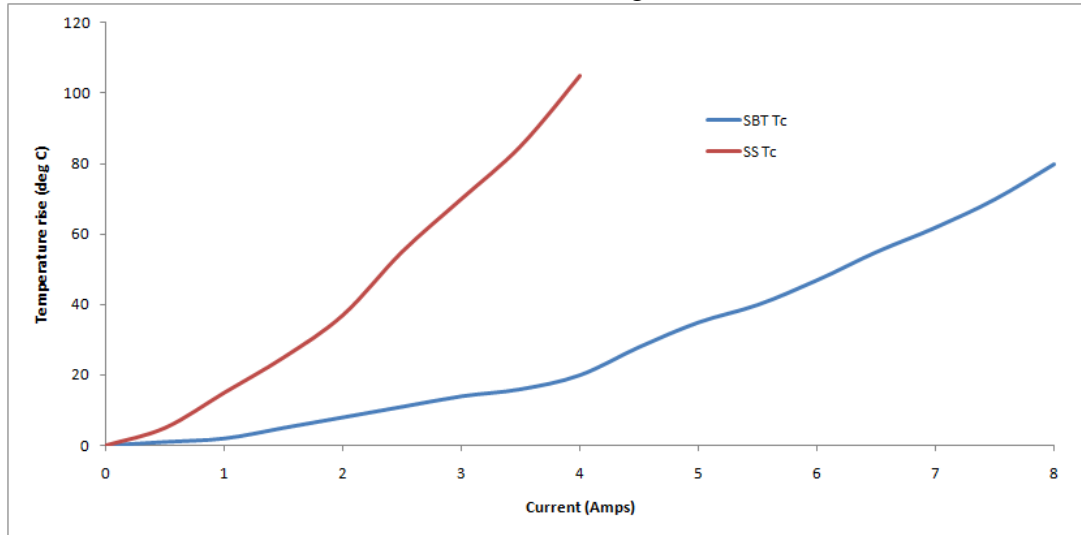
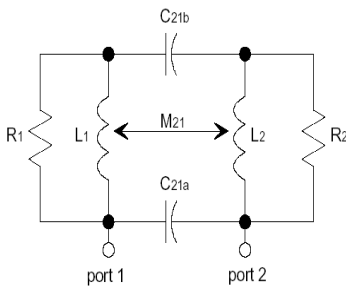


Figure 6: Temperature rise versus current carrying capacity for SS pin and SBT pin

It can be seen clearly that SBT pins can carry more current with minimal rise in temperature when compared with SS pins. This advantage of SBT pin is attributed to its physical geometry where the two components that carry current is a solid rectangular piece whereas in the SS pin, the main body is a cylindrical barrel which has less cross sectional area. This directly impacts how much current it can carry without rising temperature beyond its operating range.

High-Speed Characterization

The following test determines which contactor can handle high signal speed without loss. The spring pins with fixture was mounted onto a custom board, designed to exhibit low parasitic and allows the use of coplanar probes (for probing adjacent pins). A test chip with measurement standard pattern was mounted on top of the fixture. This setup allows pins to be measured under three conditions (open, shorted and thru). The Hewlett-Packard MDS (Microwave Design System) software was used to extract an equivalent-circuit model (Figure 7), which is SPICE compatible.



- L1, L2 : Pin self inductance
- M21 : Mutual inductance between adjacent pins
- R1, R2 : Shunt resistance of inductors L1 and L2, used to model high frequency loss due to skin effect and dielectric loss
- C21a : Mutual capacitance between adjacent pins on PCB side
- C21b : Mutual capacitance between adjacent pins on Device side
- IL : Insertion loss

Figure 7: Equivalent circuit model

All measurements were taken using a high-frequency measurement system (Hewlett-Packard 8510C network analyzer & GGB Pico-probe™ 450 mm pitch). The HP 8510C network analyzer is a frequency domain instrument. The measurements were taken as scattering parameters (a.k.a. s-parameters). The HP8510C has great calibration capabilities, which makes it the most accurate high-frequency instrument available [4].

Table 1: High speed characterization data

Pins	SBT pin data				SS pin data			
	Field	Edge	Diagonal	Corner	Field	Edge	Diagonal	Corner
L1, L2 (nH)	1.24	1.34	1.24	1.58	2.2	2.3	2.2	2.4
M21 (nH)	0.17	0.31	0.05	0.38	0.3	0.4	0.09	0.3
R1, R2 (Ω)	1000	1500	1000	800	700	700	700	700
C21a (pF)	0.025	0.032	0.004	0.063	0.03	0.04	0.005	0.05
C21b (pF)	0.055	0.064	0.008	0.067	0.06	0.09	0.01	0.05
IL (GHz)	12	14.3	NA	11.8	9.5	10	NA	9

For this work, the load-reflect-match (LRM) calibration was used. The GGB Pico-probe provides a high-quality 50 ohm path from the network analyzer and cables to the device under test. The experiment was repeated using the SBT pin and the results were shown in Table 1. The bandwidth for interconnect medium was determined from a loop-thru measurement on two adjacent pins. The nearest row of pins was grounded. The bandwidth for 1dB insertion loss is greater than 12 GHz for SBT pin. For the SS pin, the 1dB bandwidth is 9 GHz. The self-inductance (L1 & L2) values for the SBT were in the range of 1.24 to 1.58 nH. For the SS pin, the self inductance values were 2.2 to 2.4 nH. For SBT pin, the bandwidth was higher and inductance values are lower because of its solid rectangular cross sectional area even though length of both SBT and SS pins are same. Mutual inductance between adjacent pins and the capacitance values were similar for both SBT and SS pin. SBT exhibits superior results than SS pin for high speed testing.

Conclusion

A primary concern to anyone utilizing the high density devices is keeping development costs under control, optimization of existing manufacturing capability and minimizing the time-to-market. The main objective is to rely on test data and not wasting time by repetitive tests and avoid false failures. The testing conducted above solves a myriad of high-speed, high-density application needs. The test results compare the electrical and the mechanical characteristics of the two interconnection medium.

- Stamped probe provides better contact resistance than the spring probes.
- Variation of contact resistance for stamped probe is less than 3 mill ohms.
- Stamped probe has better current carrying capacity due to its solid cross sectional area for current flow path.
- Stamped probe exhibits better bandwidth for high speed signal transmission than spring probe.

Improved geometry of stamped probe eliminates cylindrical barrel and one of the constriction resistance from the network. The pinch mechanism between two solid plungers of stamped probe maintains continuity between moving components at all time and at different compression

height. This feature enables reliable test data and elimination of repetitive test steps. As time-to-market shrinks further, the main stream of the industry will embrace this technology—another step in the evolution (or revolution) of interconnection standards.

References

1. Harper, C.A., *Electronics Packaging and Interconnection Handbook*, second edition, McGraw-Hill, 1997
2. Pal, I., “Evaluating Technologies for Testing High Speed High Density Ball Grid Array Packages,” *Pan Pacific Microelectronics Symposium*, 2004.
3. Mroczkowski, R. S., and Maynard, J. M., “Estimating the Reliability of Electrical Connectors,” *IEEE Trans. on Reliability*, 1991.
4. Otonari, G., “Giga Test Labs – Spring Probe Interconnector Test Report,” May, 2006.
5. Hart, B. L., “*Digital Signal Transmission Line Circuit Technology*,” Van Nostrand Reinhold, New York, 1988.
6. Johnson, H. W., Graham, M., “*High-Speed Digital Design: A Handbook of Black Magic*,” Prentice Hall PTR, 1993.