Multi Level Stacked Socket Challenges & Solutions

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- Multi Level IC Test Need
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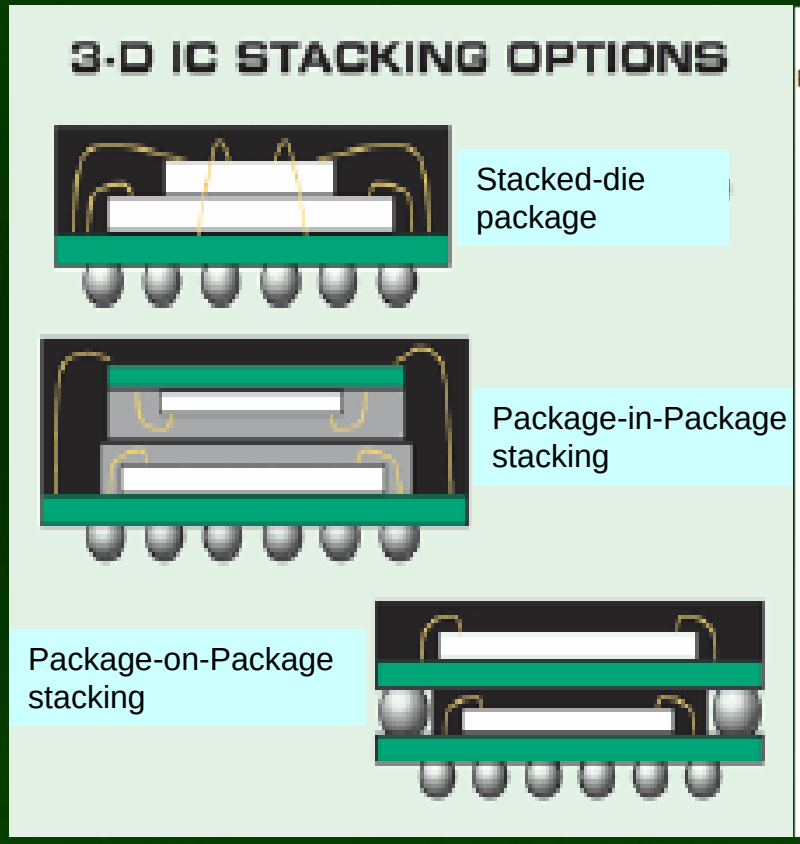
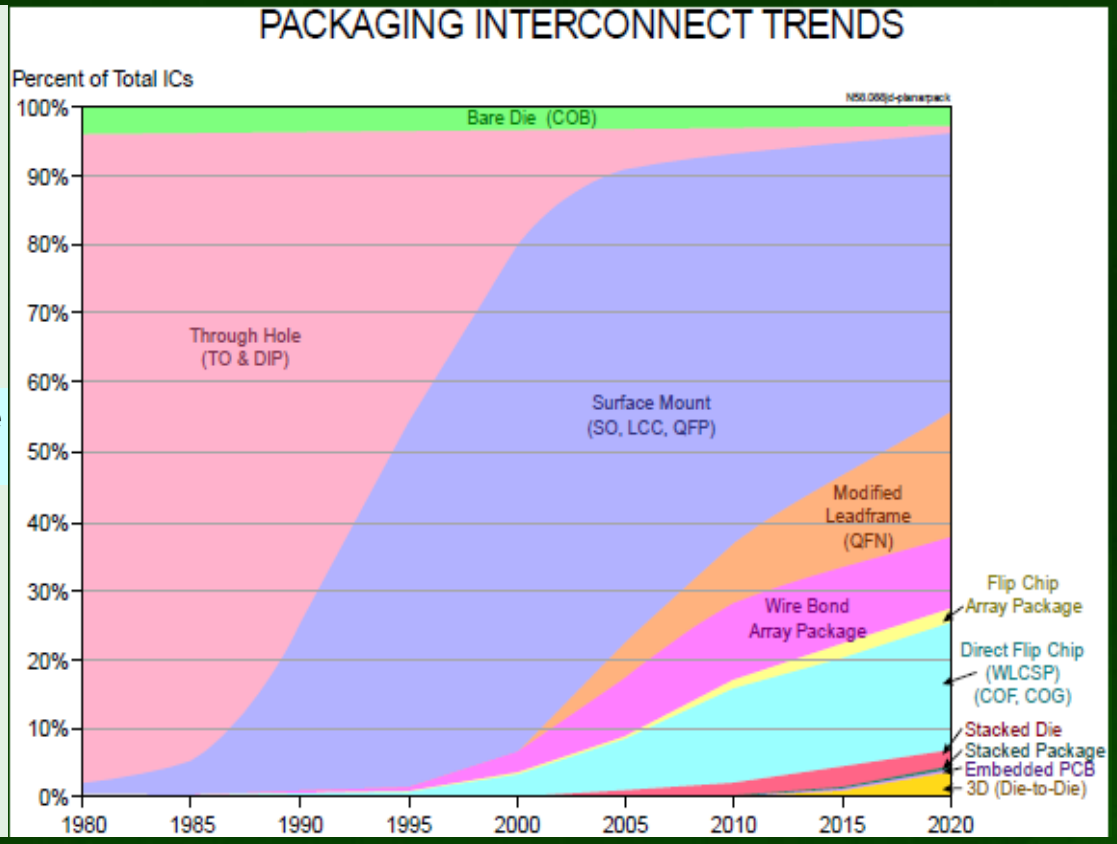
Multi Level IC Configuration & Forecast



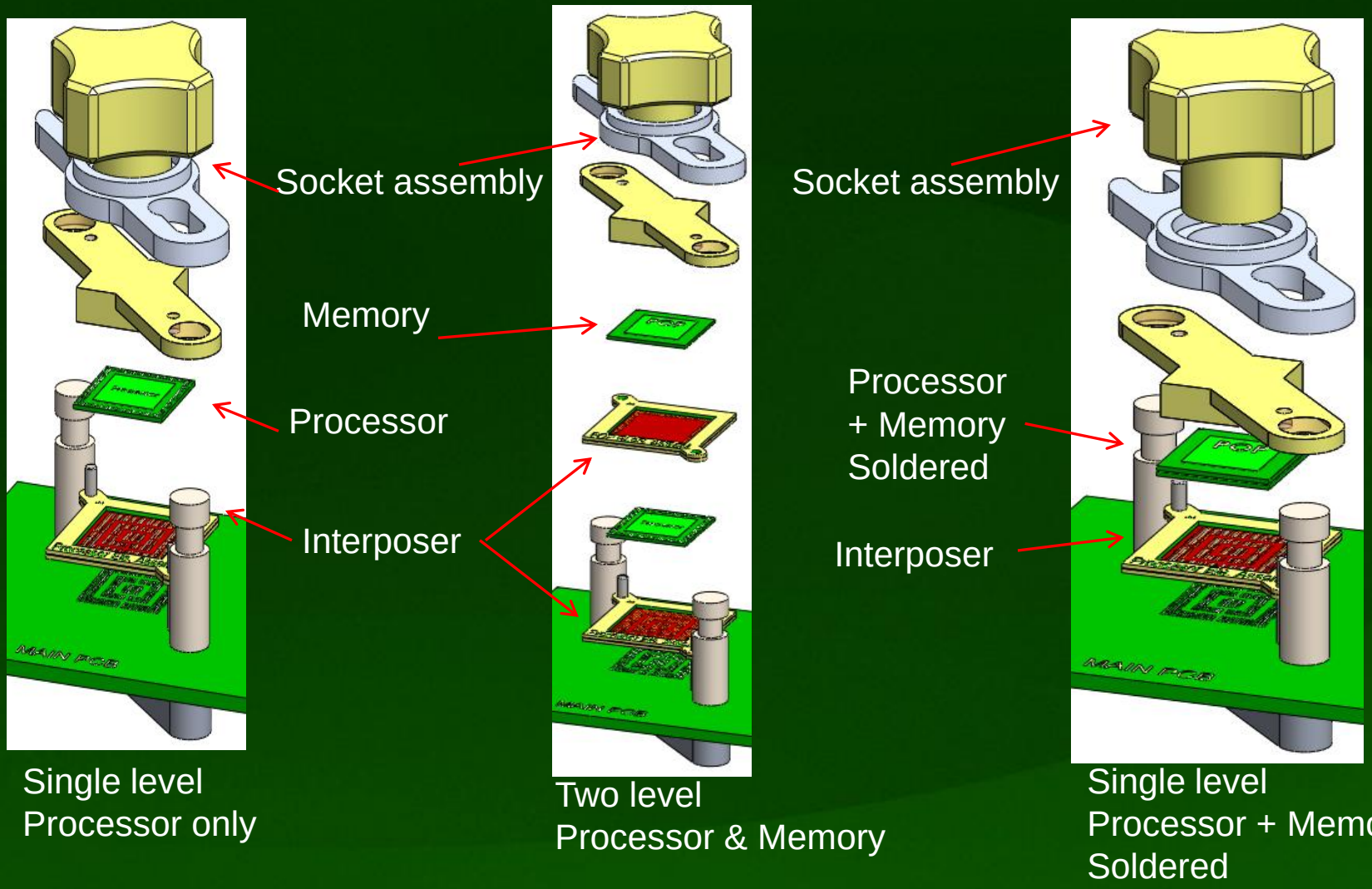


- According to Prismark, In 2020 - 3D packaging share of 7% might total well over 30 billion components that employ stacking technologies.

Multi Level IC Test Need

- Test processor by itself in a socket
- Test processor signals using a probe which is interfaced between processor and target PCB
- Test processor with memory soldered
- Test processor with replaceable memory
- Test memory signals using a probe which is interfaced between memory and processor
- Test memory signals and processor signals using memory probe and processor probe in the stack up between memory and processor on target PCB

Multi Level IC Socket Configuration

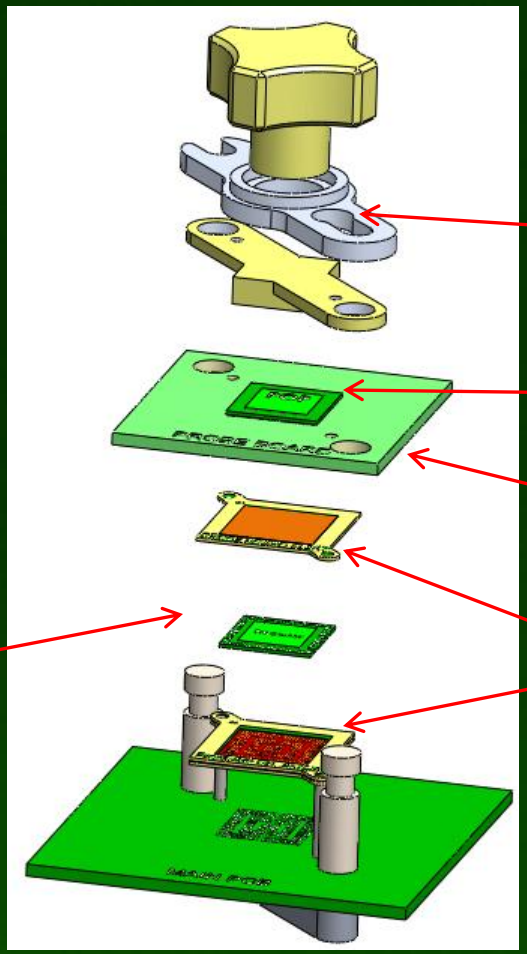


Single level
Processor only

Two level
Processor & Memory

Single level
Processor + Memory
Soldered

Multi Level IC Socket Configuration



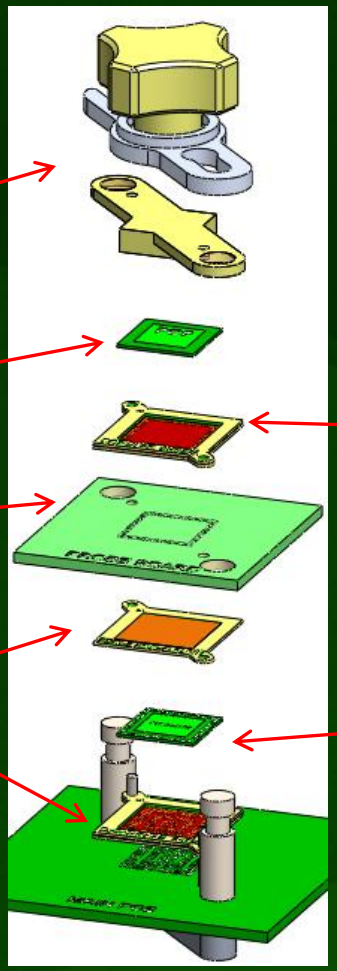
Socket assembly

Memory

Memory probe

Processor

Interposer



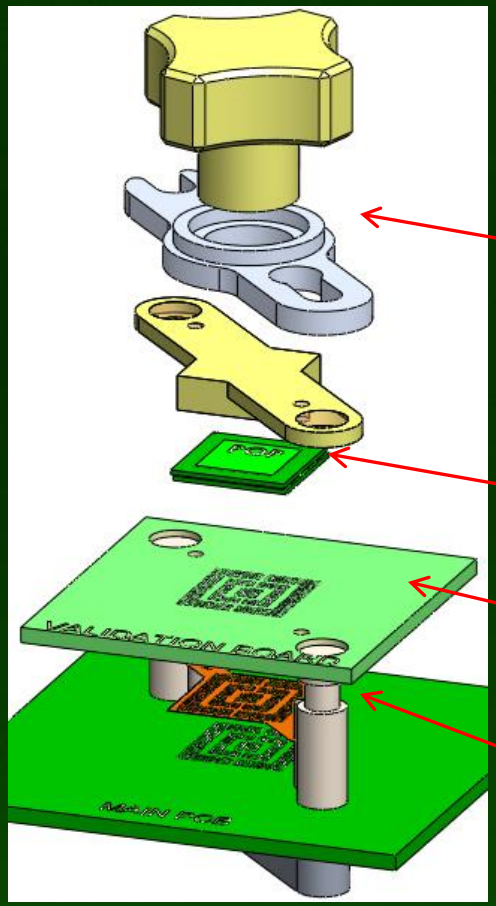
Interposer

Processor

Two level
Processor & Memory probe

Three level
Processor, Memory probe & Memory

Multi Level IC Socket Configuration



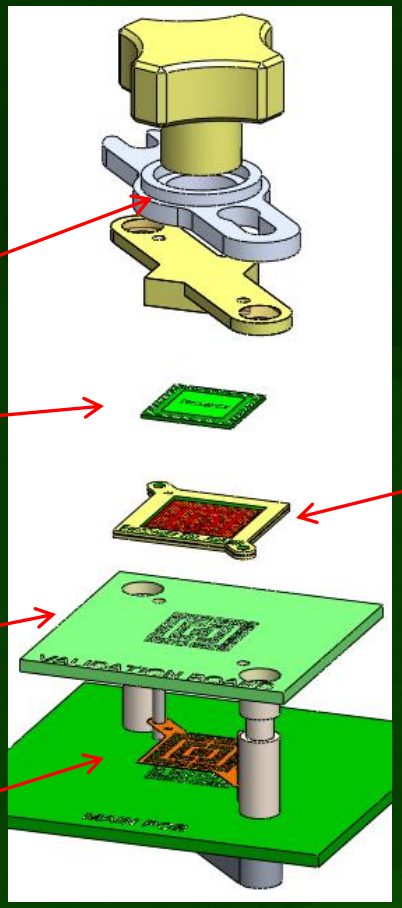
Socket assembly

Processor

Processor +
Memory soldered

Processor probe

Interposer

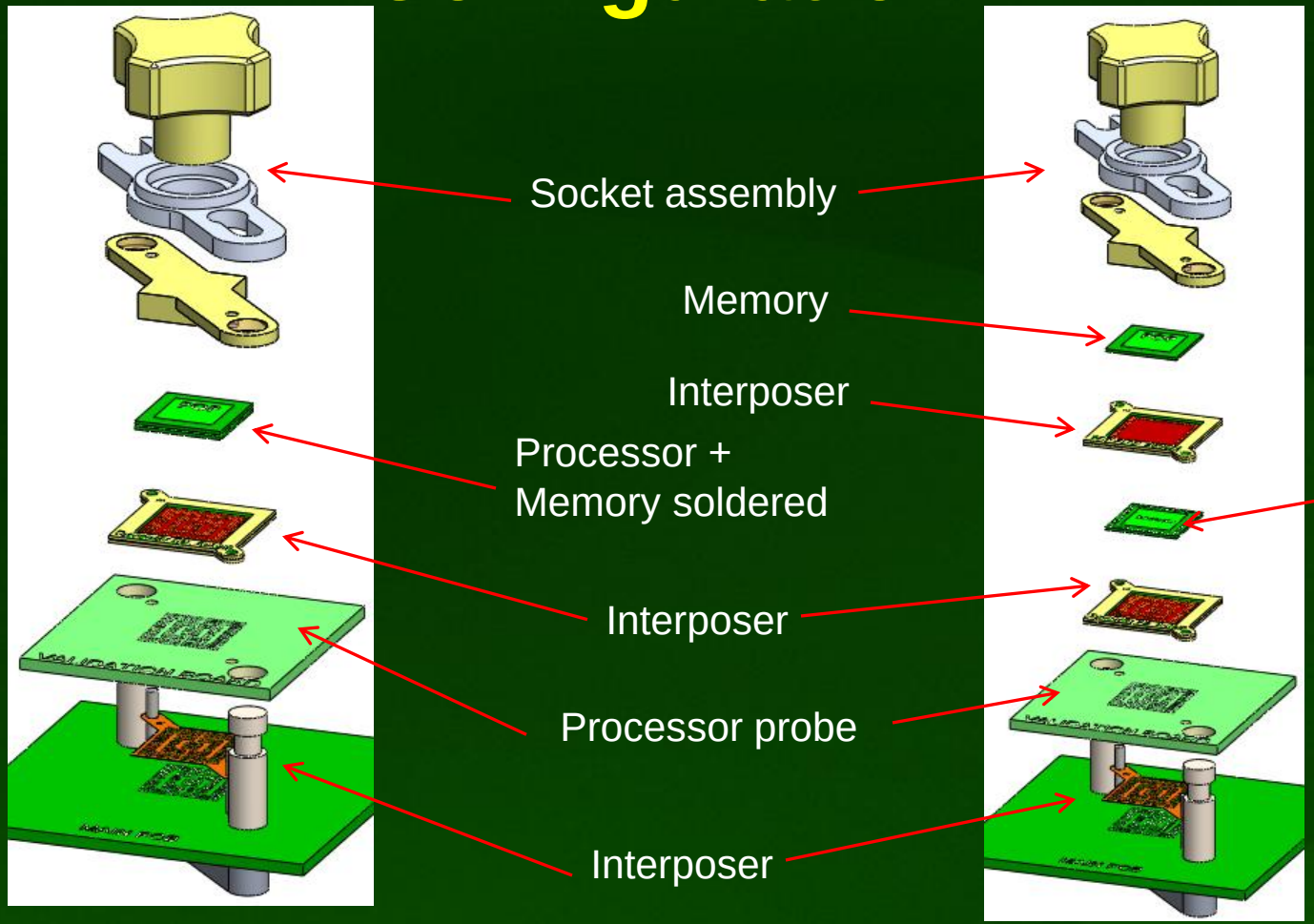


Interposer

Single level
Processor soldered on probe

Two level
Processor & Processor probe

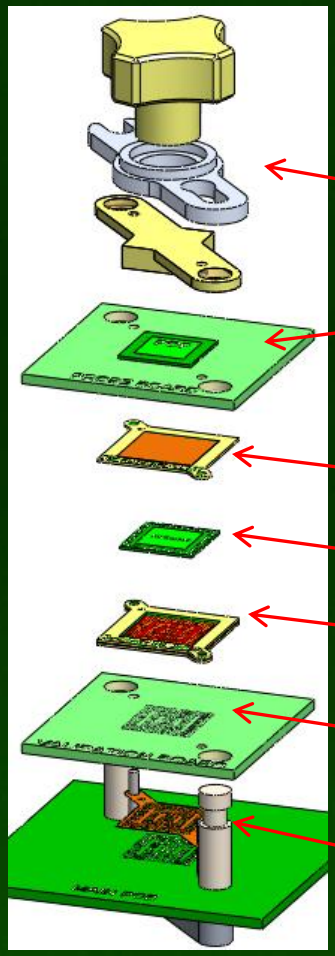
Multi Level IC Socket Configuration



Two level
PoP & Processor probe

Three level
Processor, Memory & Processor probe

Multi Level IC Socket Configuration



Socket assembly

Memory Soldered to Probe

Interposer

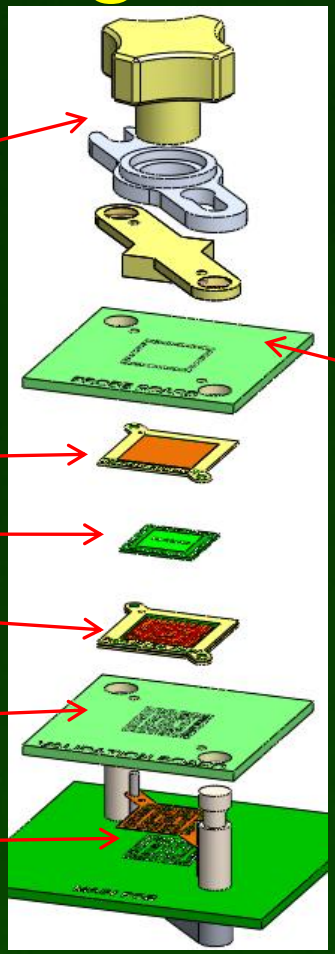
Processor

Interposer

Processor probe

Interposer

Three level
Memory soldered probe,
Processor & Processor probe



Three level
Memory probe, Processor
& Processor probe

Socket assembly

Memory

Interposer

Memory probe

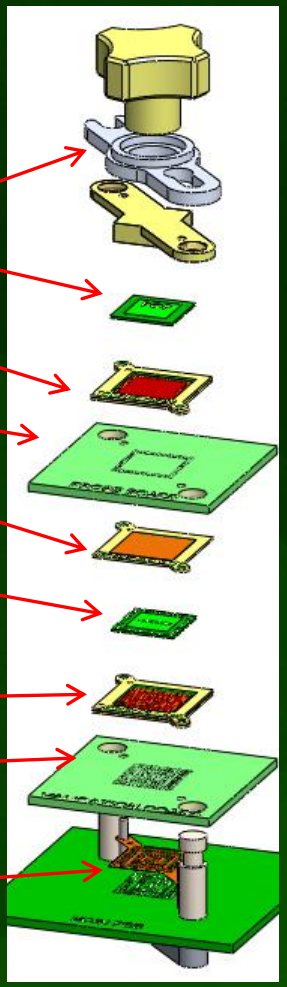
Interposer

Processor

Interposer

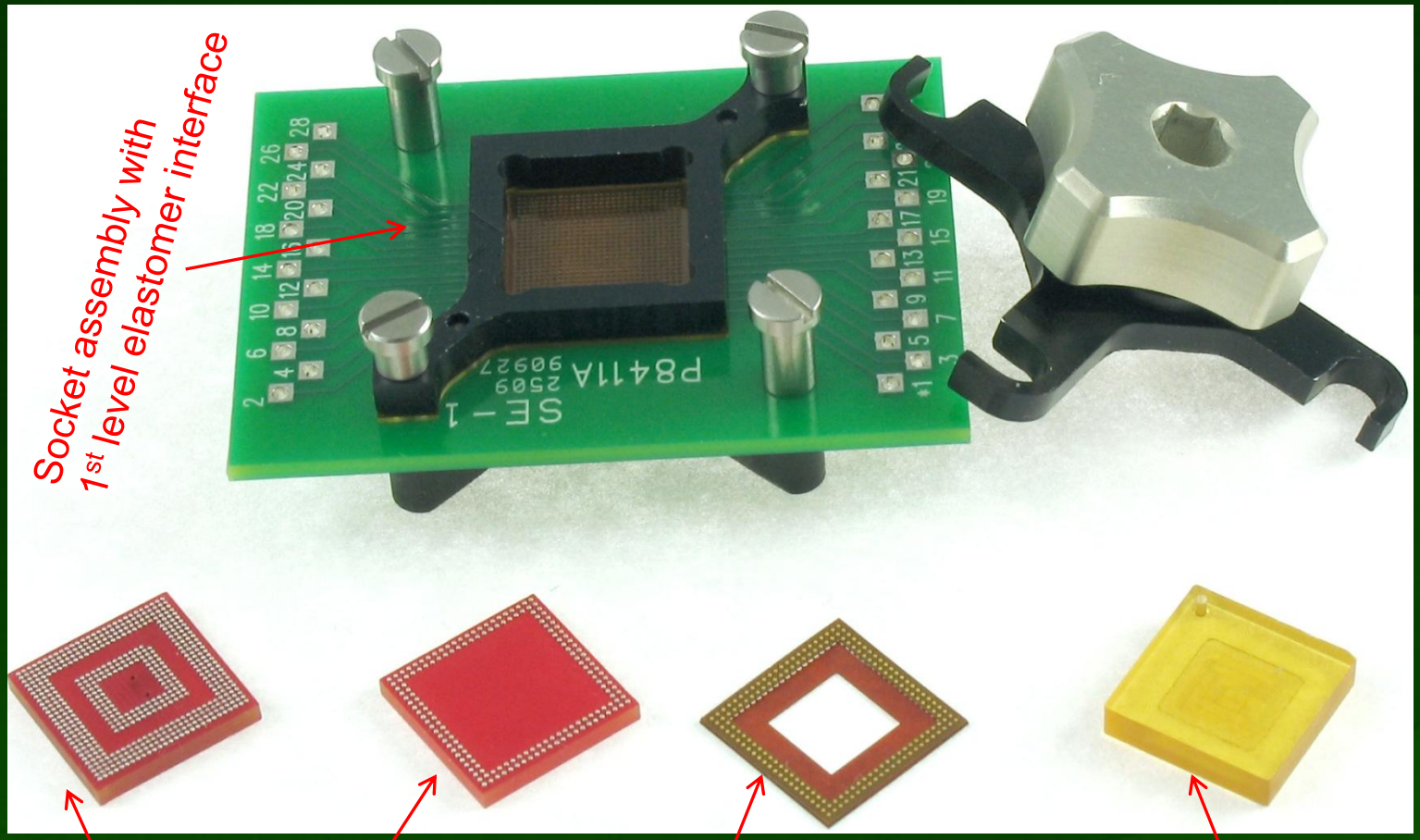
Processor probe

Interposer

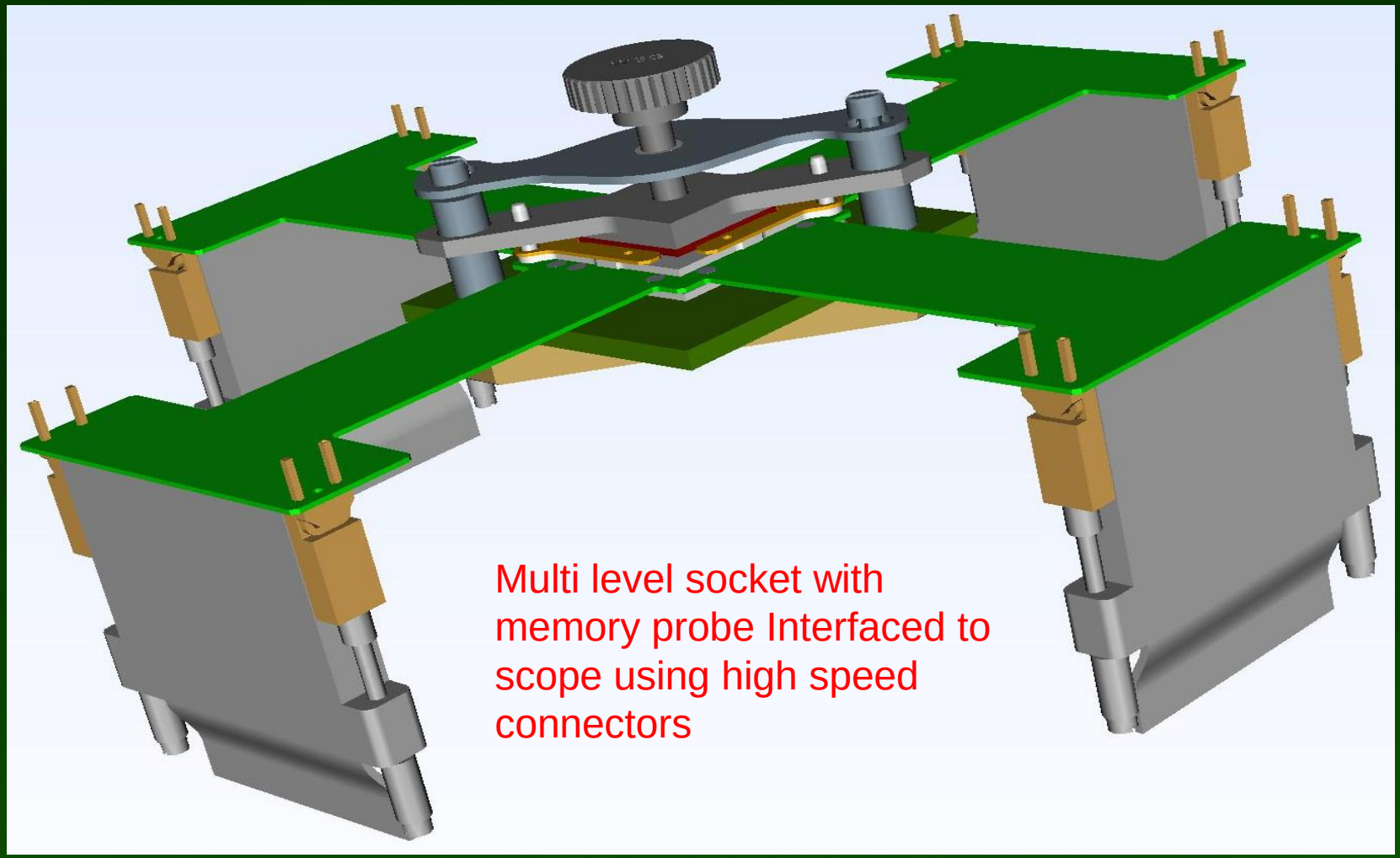


Four level
Memory, Memory probe
Processor & Processor probe

Multi Level IC Socket Configuration



Multi Level IC Socket Electrical Challenges

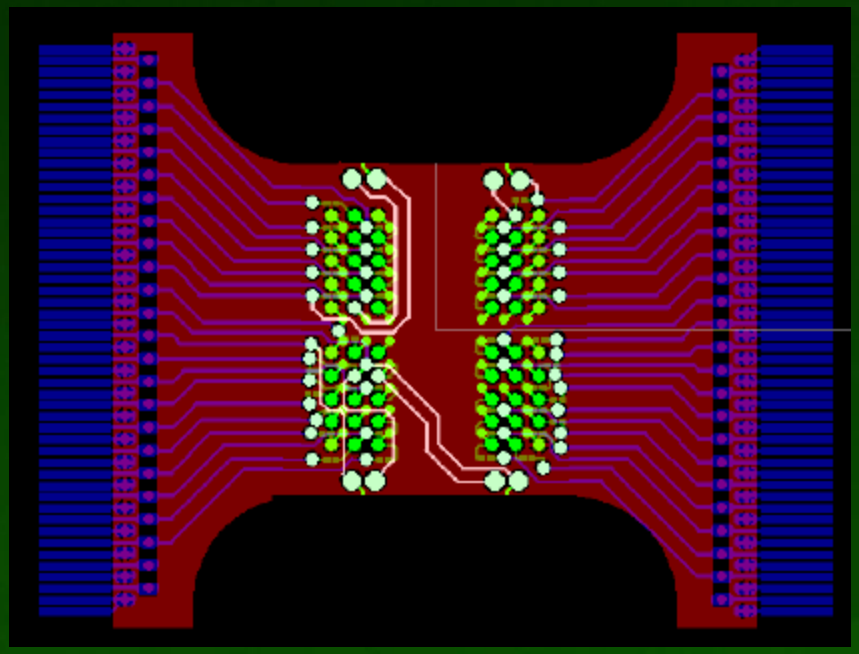


Source: Texas Instruments

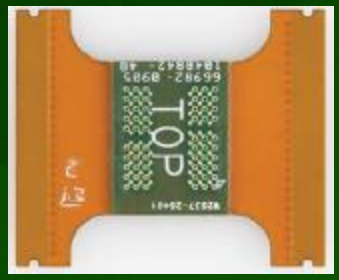
Multi Level IC Socket Electrical Challenges

Four wing probe for DDR memory

Two wing probe for DDR memory under test



Two wing probe for DDR memory with optimized signal routing

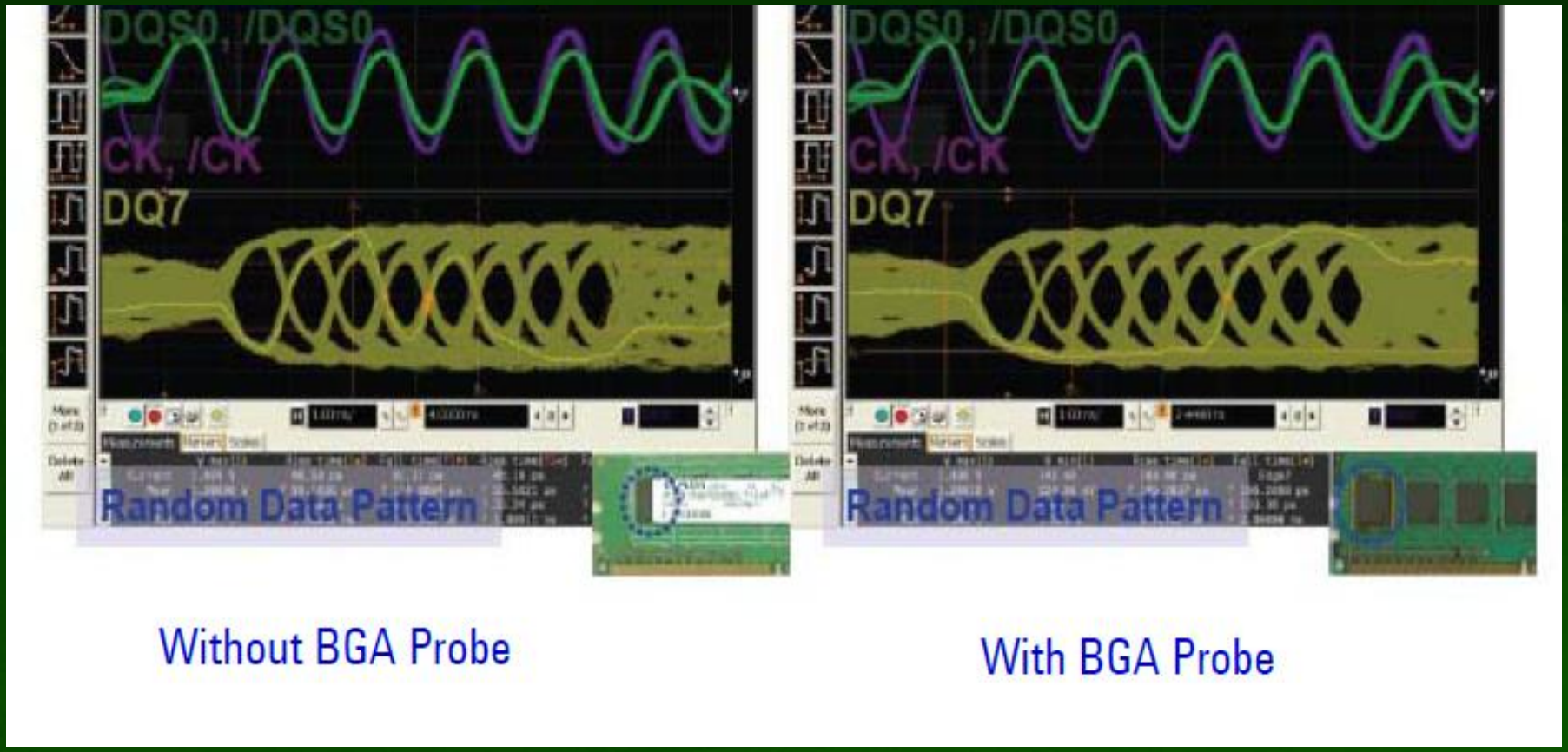


Source: Agilent Technologies

Electrically Transparent Probing

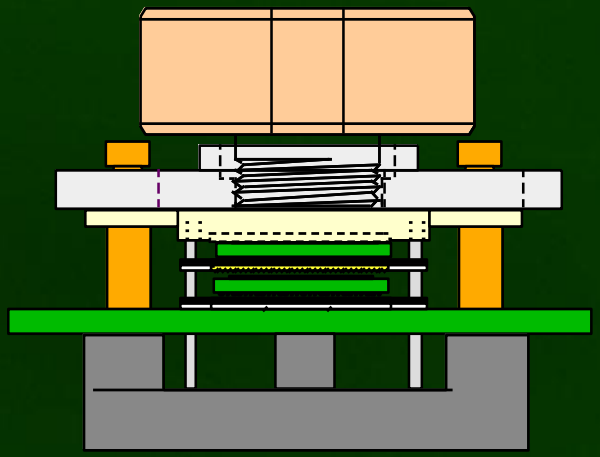
Without interposer

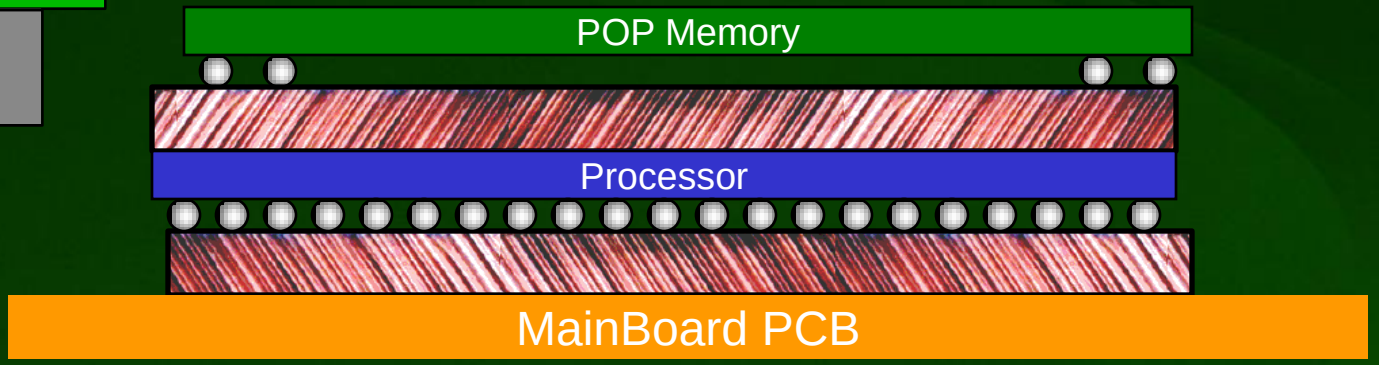
With interposer



Source: Agilent Technologies

Multi Level Stack Up Alignment Challenges

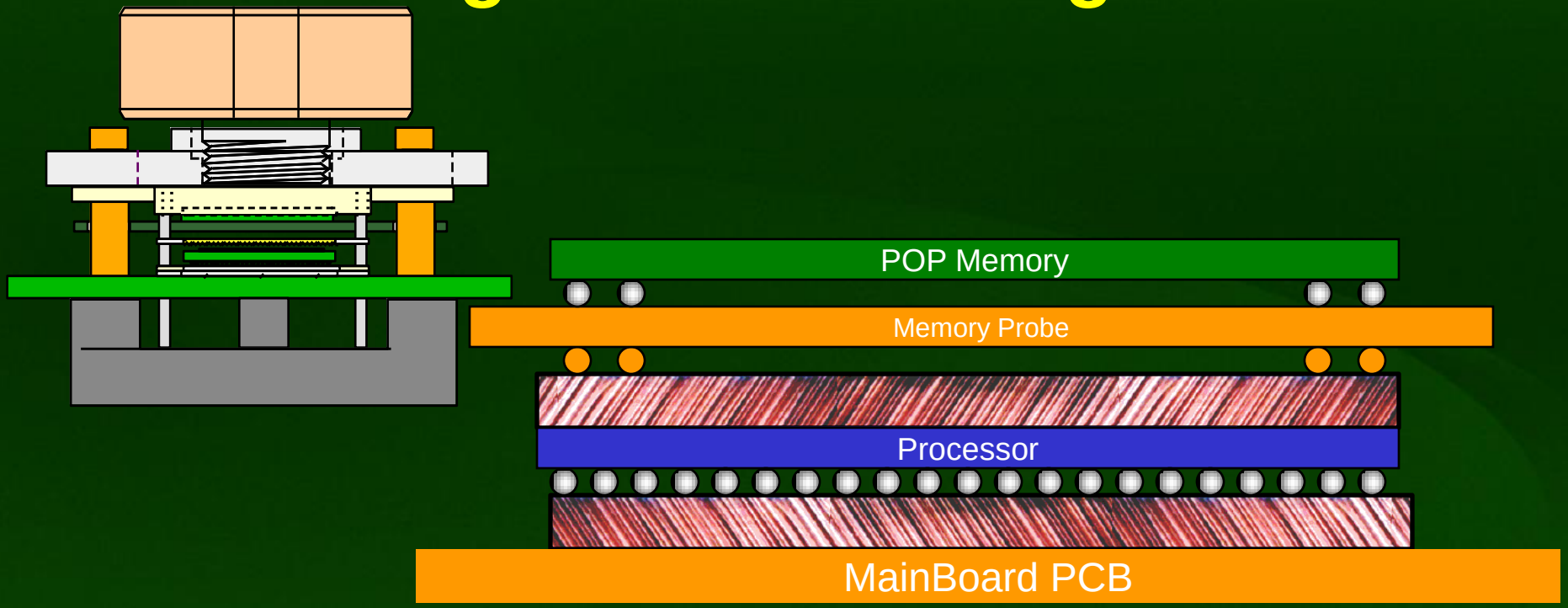




Configuration 1: Processor and Memory

1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Memory will be centered on the Ball guide and IC guide.

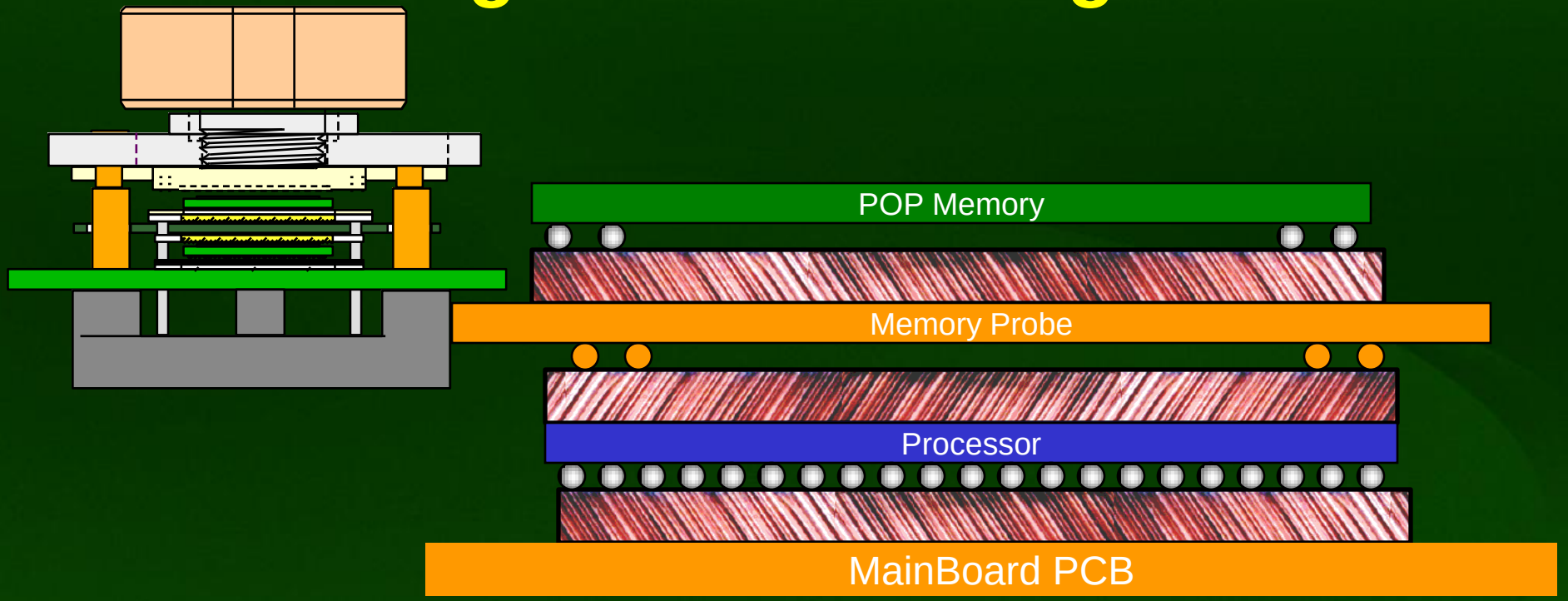
Multi Level Stack Up Alignment Challenges



Configuration 2: Processor and Memory Probe

1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Memory probe will be centered.

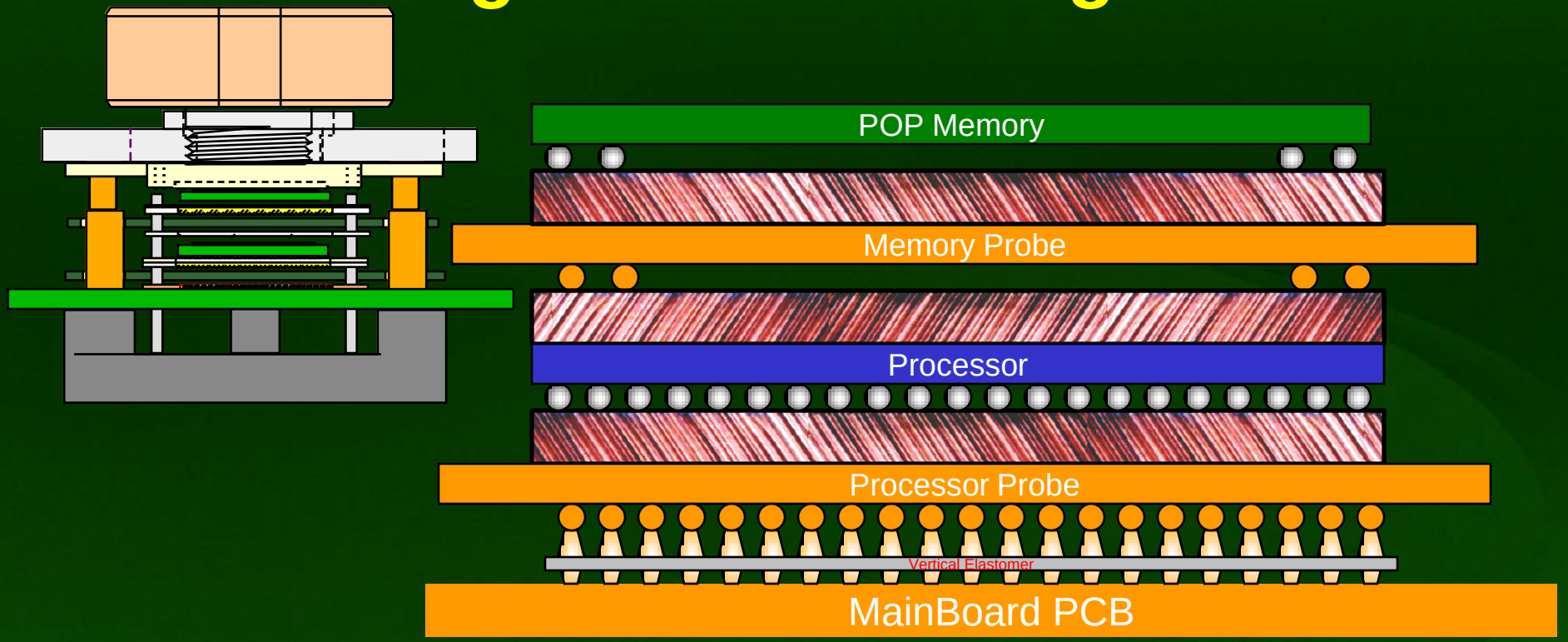
Multi Level Stack Up Alignment Challenges



Configuration 3: Processor, Probe board and Memory

1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Probe board will be centered.
3. PoP memory is shifted 0.25mm to left with IC guide and Ball guide.

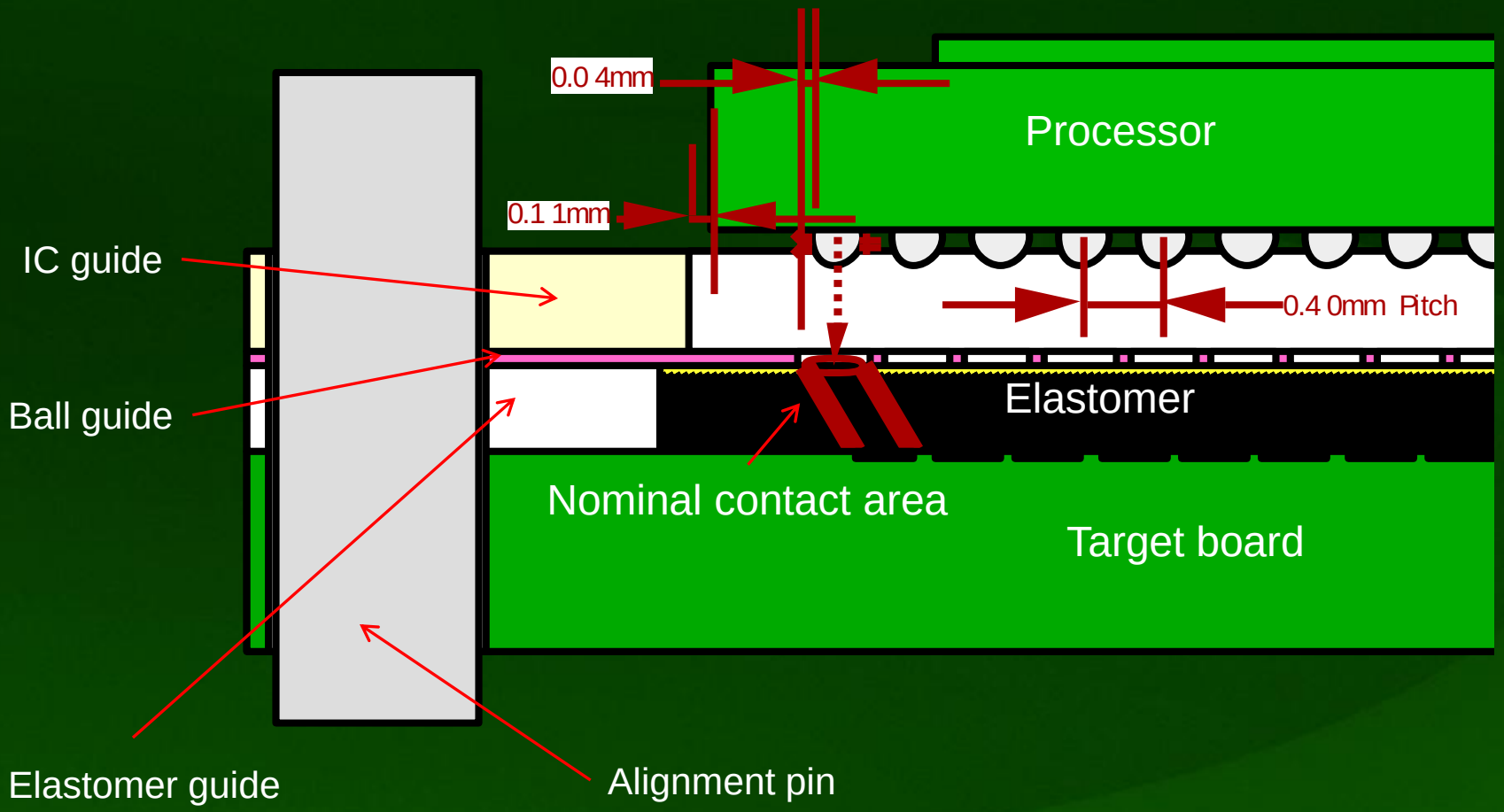
Multi Level Stack Up Alignment Challenges



Configuration 4: Processor Probe, Processor, Memory Probe and PoP

1. Processor and POP sits 0.25mm shifted with pattern on target board. Processor probe and memory probe sits centered with respect to target board.
2. Vertical elastomer on first layer.

Multi Level Stack Up Alignment Challenges



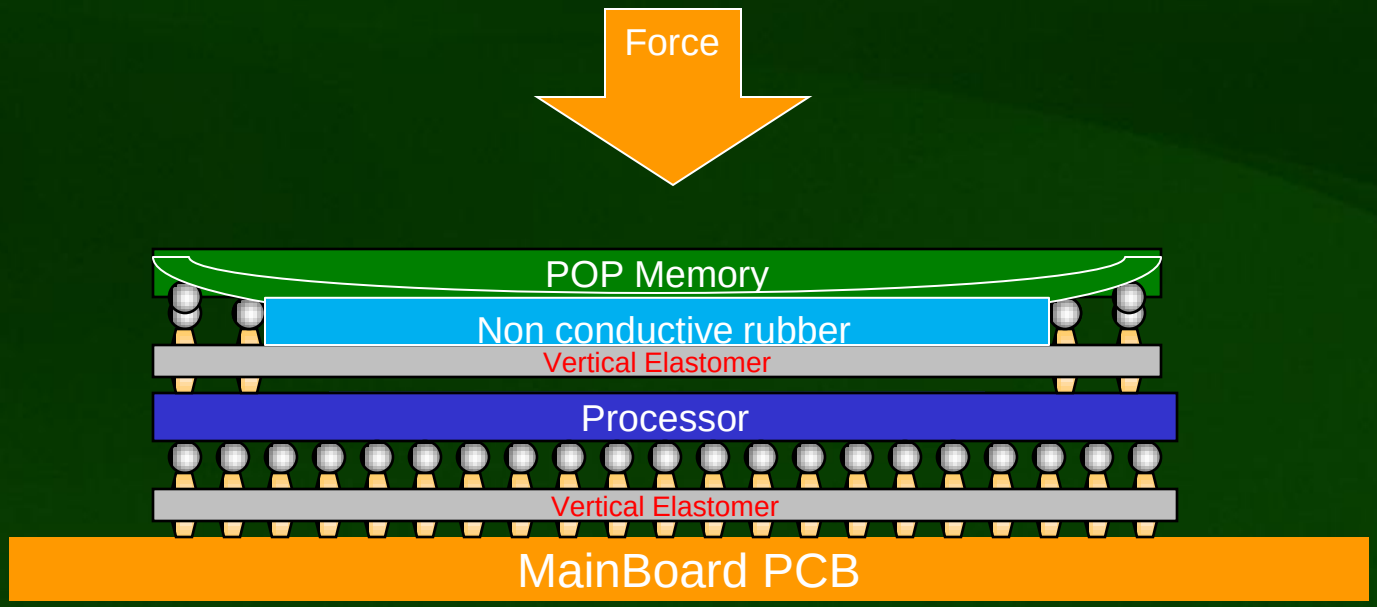
Multi Level Stack Up Alignment Challenges

Processor/Elastomer/PCB tolerance	:	±
PCB Alignment Hole position	:	+0.025mm
Ball guide Alignment Hole position	:	+0.025mm
PCB Pad location/Size	:	+0.05mm

=0.1mm off from nominal location

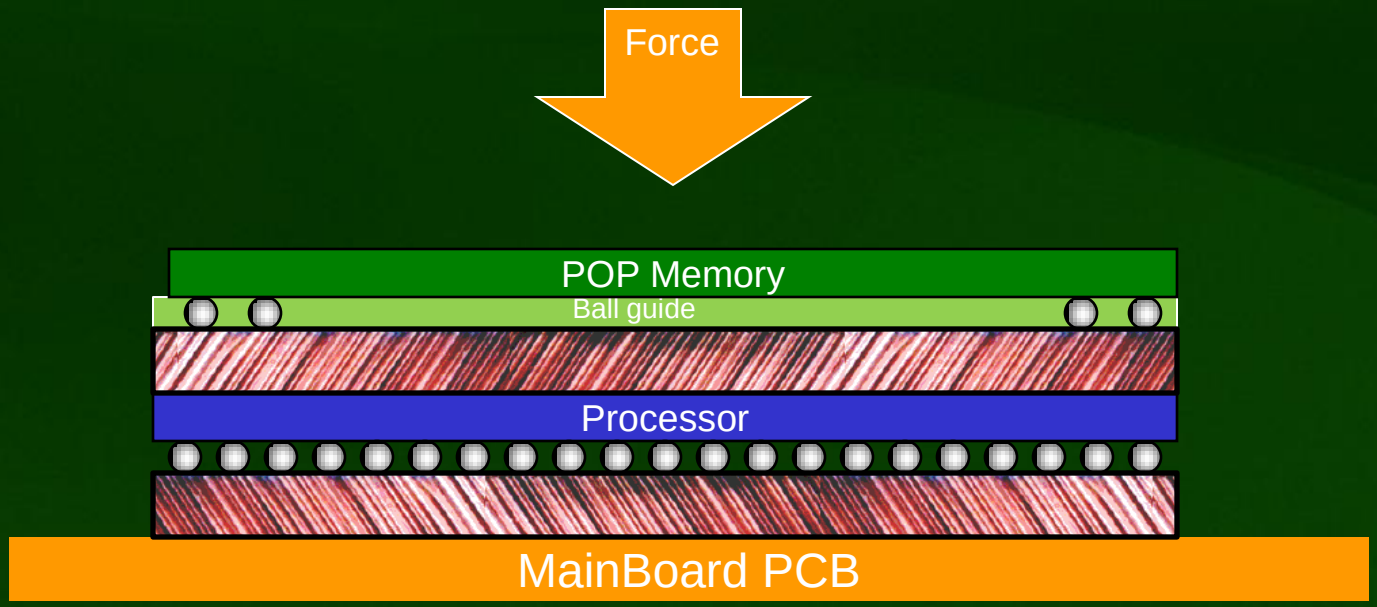
With 0.24mm minimum pad diameter for 0.4mm pitch BGA, elastomer contacts more then 58% of the pad. This XY variation occurs on each level of the stack up. Similar calculations were made for Z variations and manufacturing tolerances were updated such that 60% of pad is covered by elastomer.

Multi Level Stack Up Force Challenges



Force balance using additional non-conductive rubber

Multi Level Stack Up Force Challenges



- Force balance using angled interposer itself
- Shift allows normal force to be lower than vertical interposer

Multi Level Stack Up Force Challenges

- Force data for a four level interconnect stack up shown as per ball count
- Series network of forces are balanced at each level either by using an additional non-conductive rubber or elastomer by itself

	Elastomer	Ball Count	Force/Ball, gm	Total Force, Kg
PoP Memory Probe	Angle	169	30	5.07
Memory Probe Processor	Angle	169	30	5.07
Processor Processor Probe	Angle	515	30	15.45
Processor Probe Target Board	Straight	515	35	18.025

Conclusion

- 3D packages are the future
- Pitch, pin count , performance complexities increase due to consumer demand
- Two level package needs four level interconnect for development
- XYZ alignment challenges in each interconnect level push manufacturing capabilities to its extreme
- Force balancing at each level enables innovative design and requires new materials with unique properties